

MODEL NAME : VAW11
PROJECT CODE : ANRVAW1100
PCB NO : LA-9102P (Mars Pro)
DA60000UU00 LA-9102P M/B
DA40001G400 LS-9105P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B
DA40001FR00 LS-9104P ODD/B

Dell / Compal Confidential

Schematic Document

Intel Chief River

Ivy Bridge(BGA) + Panther Point

OAK 17" UMA/DIS AMD Mars Pro

2012-09-25
Rev: 1.0

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

KB9012@ : ENE KB9012 Implemented

UMA@ : Only for UMA

EMC@ : EMI/ESD parts

GCLK@ : Green CLK implemented

GCLKUMA@ : Green CLK for UMA

GCLKDIS@ : Green CLK for DIS

XTAL@ : X'tal implemented

XTALDIS@ : X'tal with DIS implemented

R1@ : R1 P/N

R3@ : R3 P/N

i3R1@ : CPU i3-3217 1.8G

i3VOSR1@ : CPU i3-2365 1.4G

i5R1@ : CPU i5-3317 1.7G

i7R1@ : CPU i7-3517 1.9G

CEL1@ : CPU Celeron 887 1.5G

PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete

TH@/THR1@ : Thames-XT

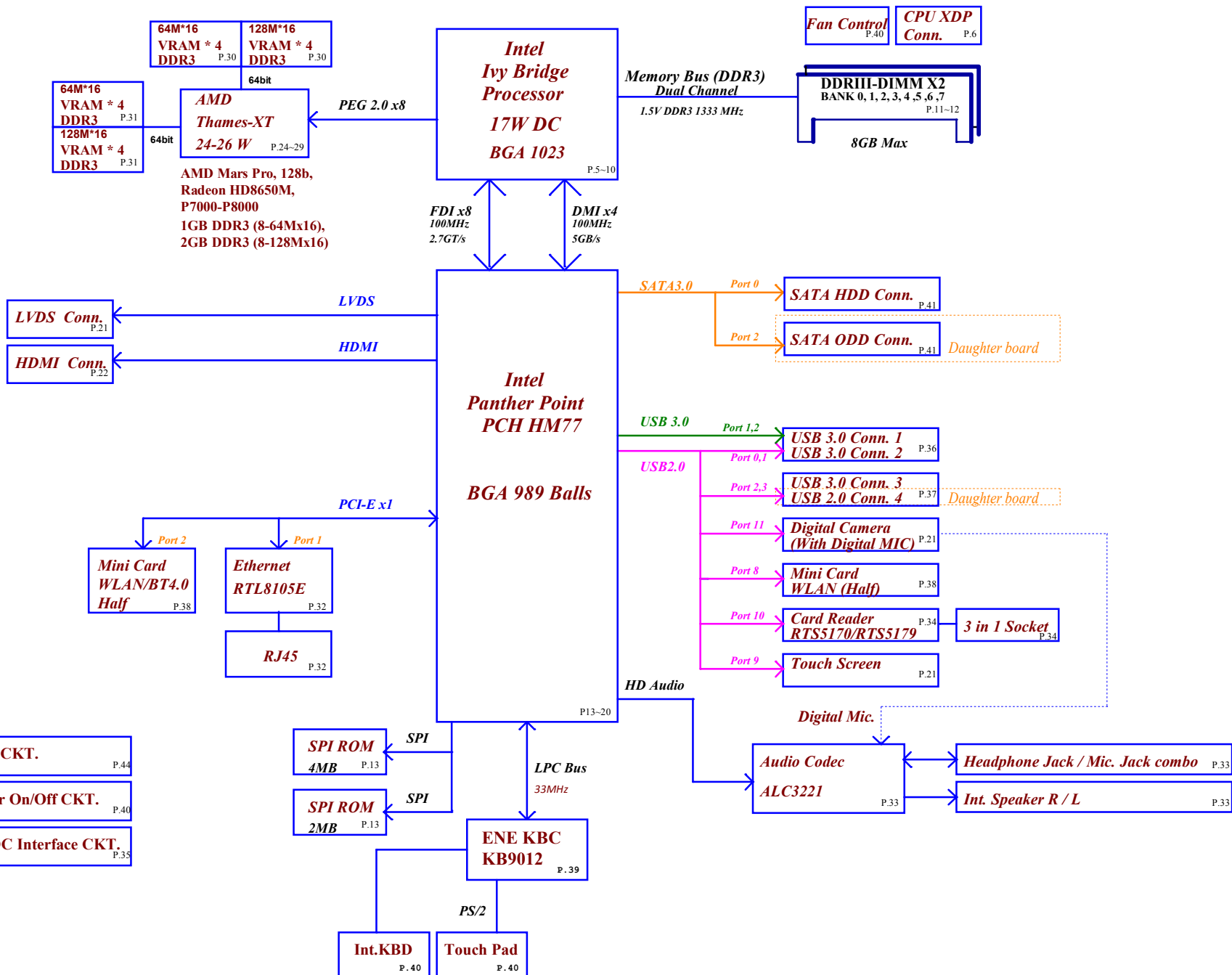
MS@/MSR1@ : Mars Pro

X76@ :

SPI-ROM & VRAM Group

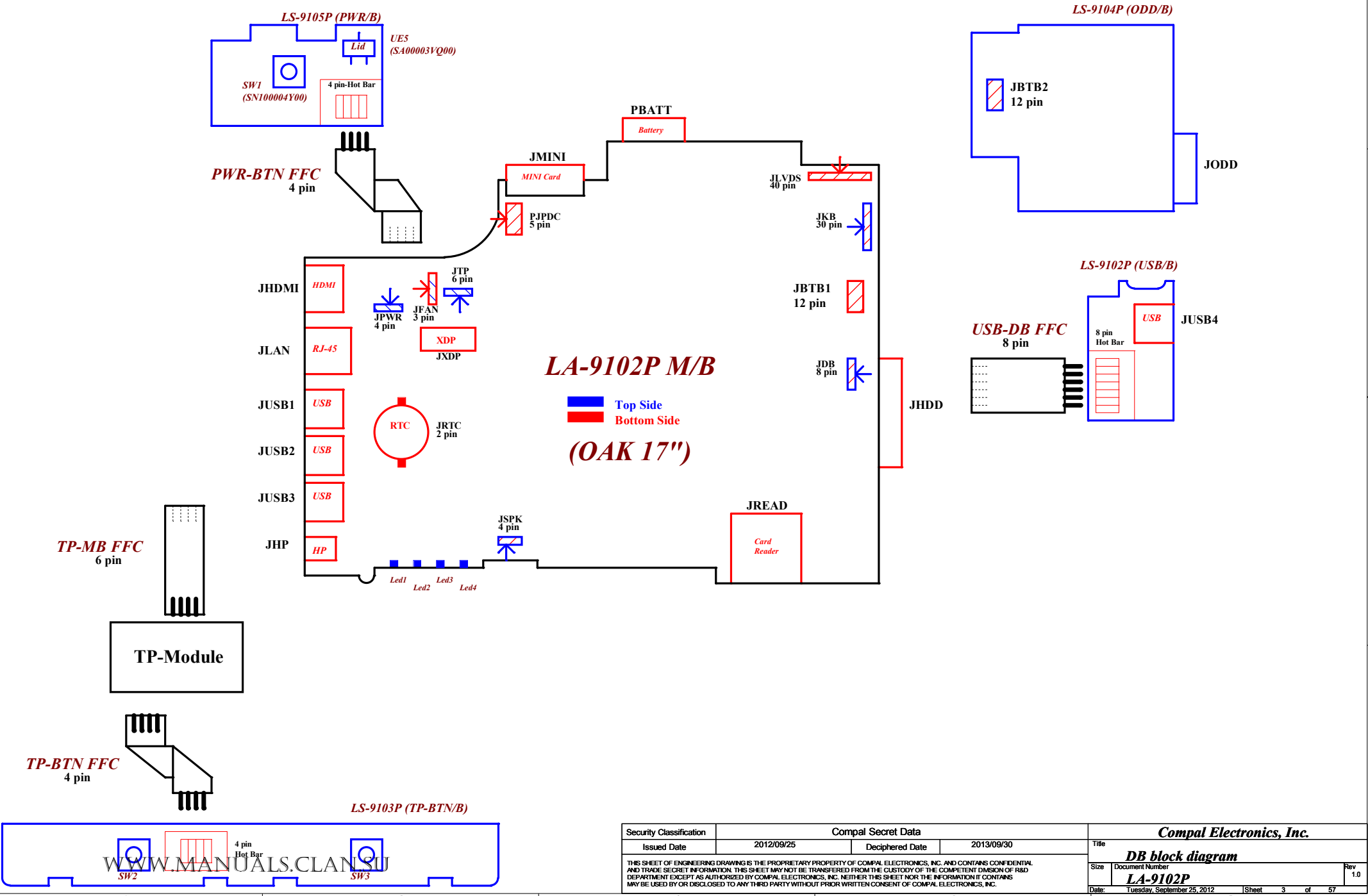


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Project Code : VAW11
File Name : LA-9102P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

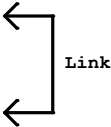
ID	PCB Revision
0	0.1
1	0.1
2	0.2
3	0.2
4	0.3
5	0.3
6	1.0
7	1.0
UMA	THM
MARS	

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	



CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

PCH	USB PORT#	DESTINATION
	0	USB conn.2
	1	USB conn.1
	2	USB conn.3
	3	USB conn.4 (DB)
	4	NC
	5	NC
	6	NC
	7	NC
	8	MINI CARD (WLAN)
	9	NC
	10	Card Reader
	11	Camera
	12	NC
	13	NC

Symbol Note :

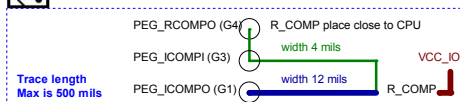


: means Digital Ground

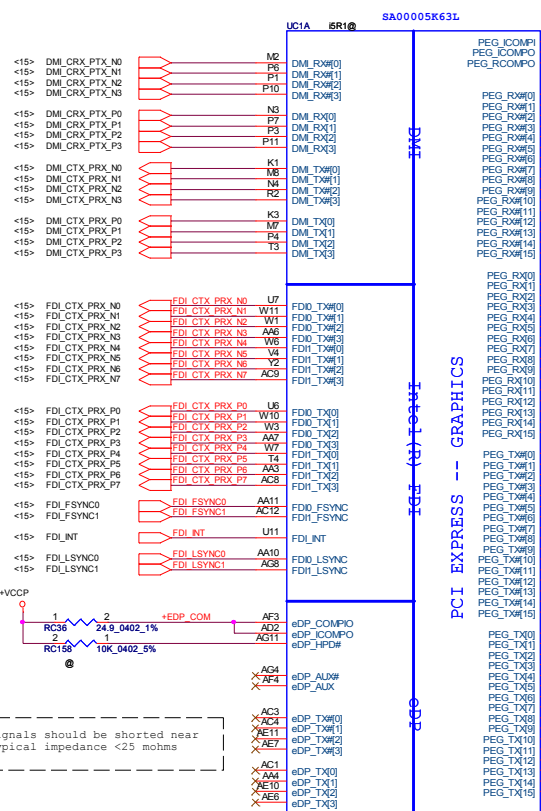


: means Analog Ground

- (1) PEG_RCOMP0 (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC1.
(2) PEG_ICOMPO use 12mil connect to RC1



PEG_ICOMPI and RCOMP0 signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



PCI EXPRESS -- GRAPHICS

PCI EXPRESS

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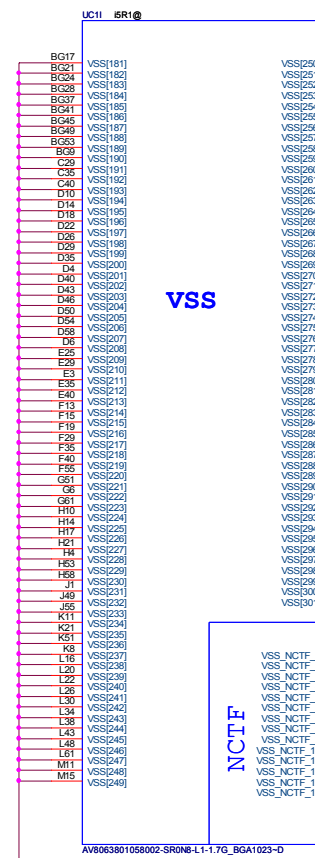
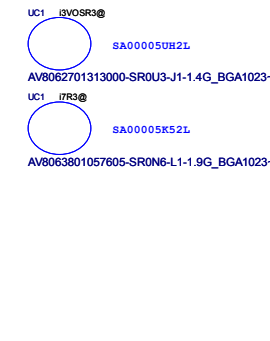
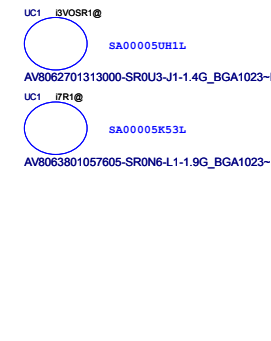
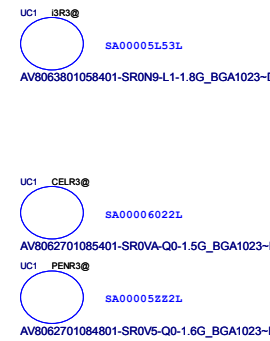
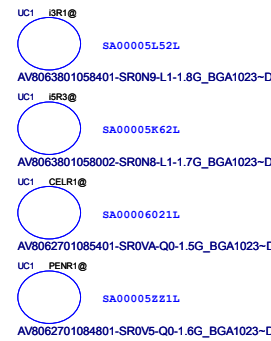
GRAPHICS

PCI EXPRESS

GRAPHICS

PCI EXPRESS

GRAPHICS



VSS

NCTF

RC20

1K_0402_5%

RC20

1K_0402_5%

RC20

1K_0402_5%

RC20

1K_0402_5%

RC20

1K_0402_5%

RC20

1K_0402_5%

RC20

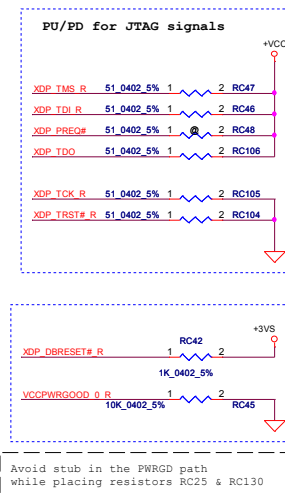
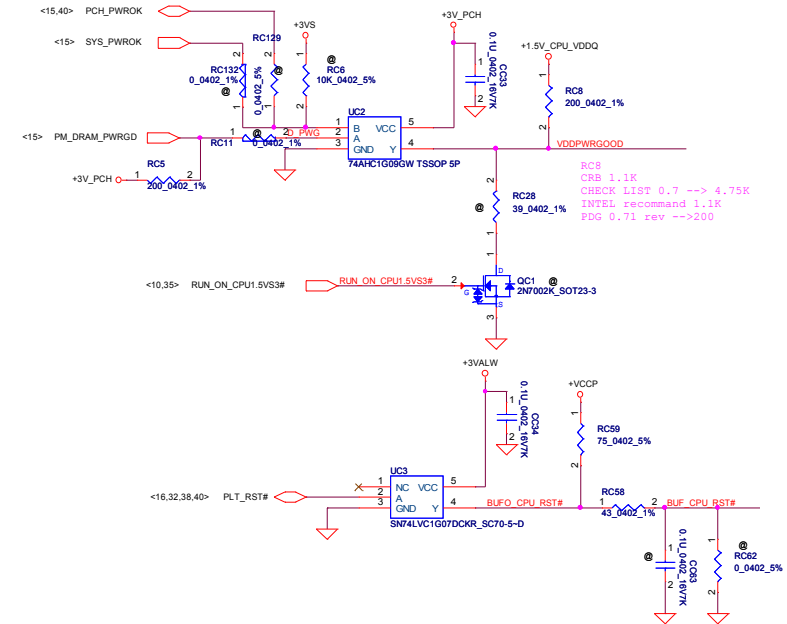
1K_0402_5%

RC20

1K_0402_5%

RC20

1K_0402_5%



PEG Static Lane Reversal - CFG2 is for the 16x

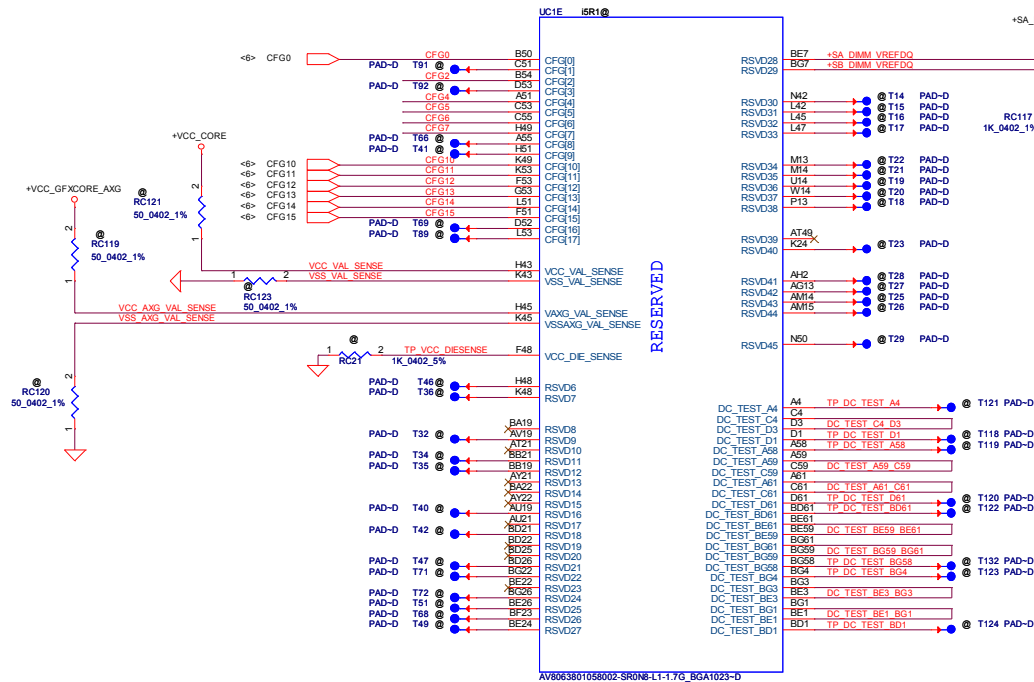
CFG2	<p>1: (Default) Normal Operation; Lane # definition matches socket pin map definition</p> <p>*0: Lane Reversed</p>
------	--

Display Port Presence Strap

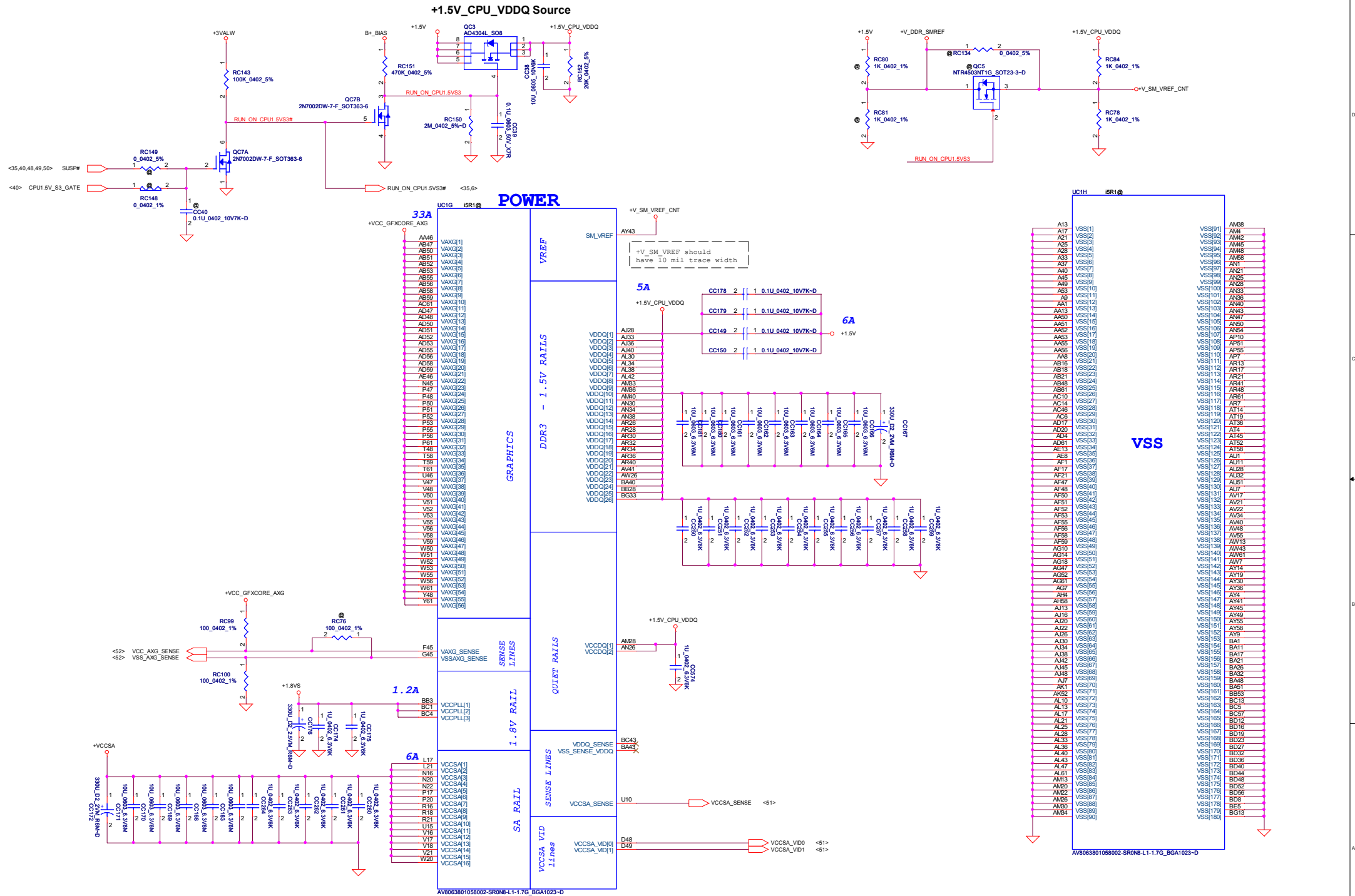
CFG4	<p>* 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device connected to the Embedded Display Port</p>
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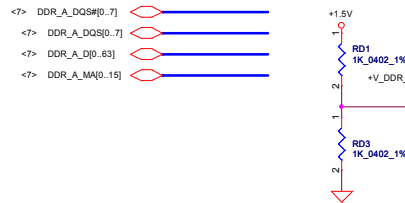
PCIe Port Bifurcation Straps

CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 enabled</p> <p>*10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled; function 2 enabled)</p> <p>00: x8, x4, x4 - Device 1 functions 1 and 2 enabled</p>
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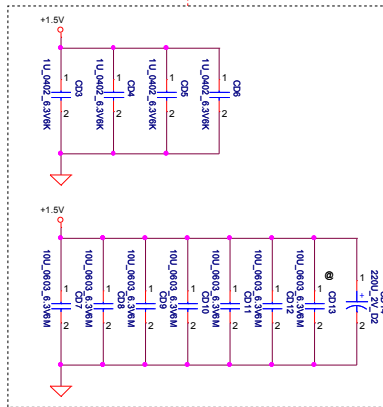
PEG DEFER TRAINING	
CFG7	<p>*1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



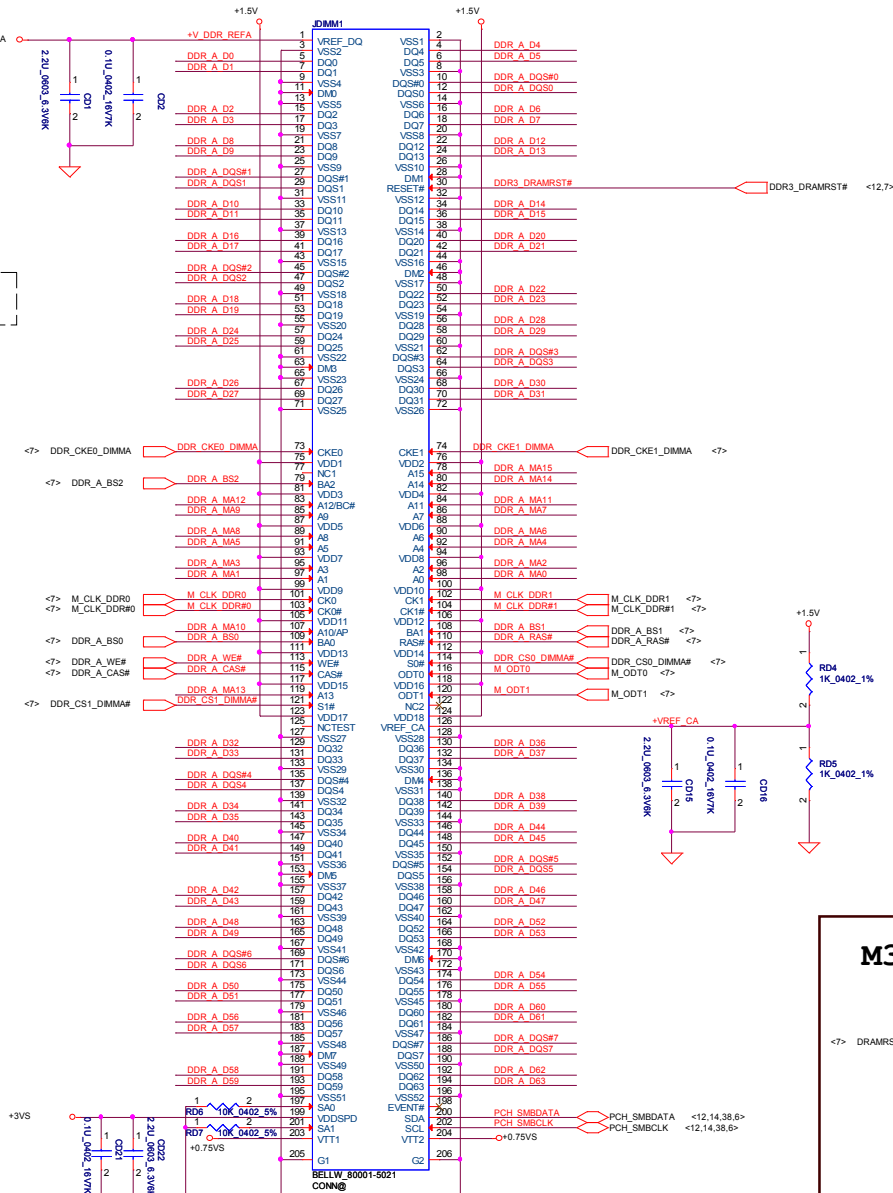
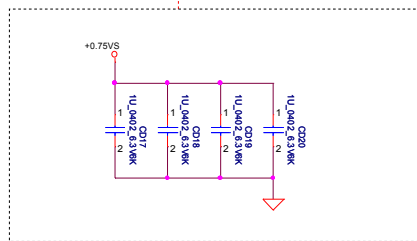


Layout Note:
Place near JDIMM1

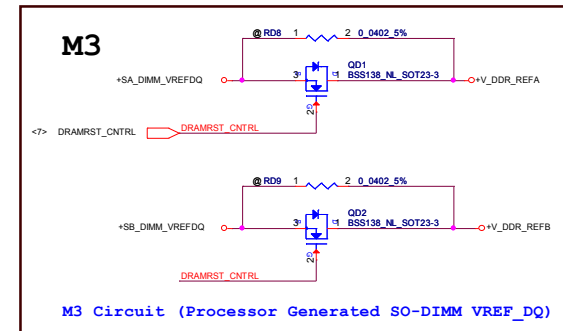
All VREF traces should have 10 mil trace width

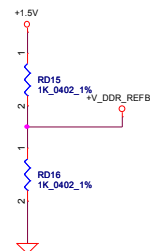


Layout Note:
Place near JDIMM1.203,204

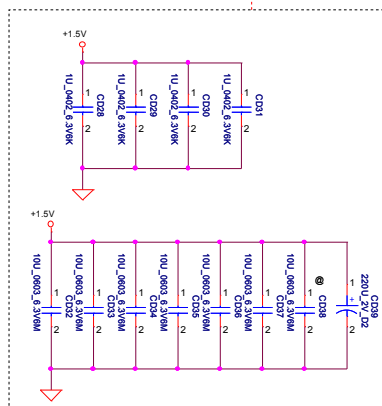


SP07000L200



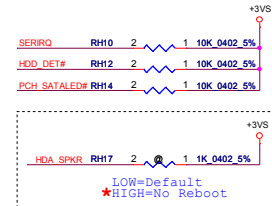
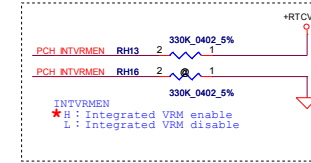
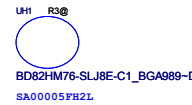
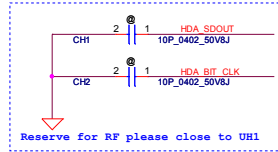
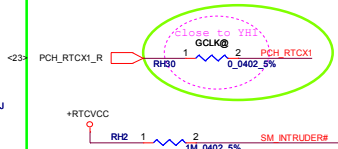
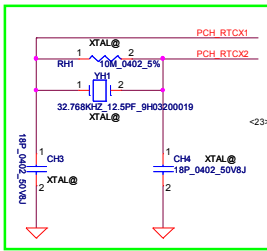


| All VREF traces should
| have 10 mil trace width

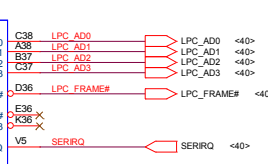
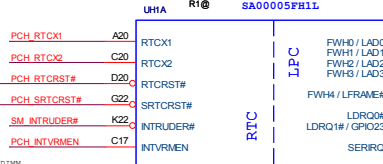
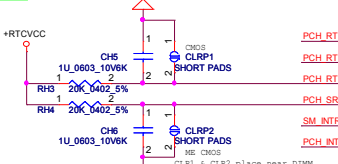


WWW.MANUALS.CLAN.SU

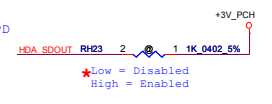
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keep away hot spot

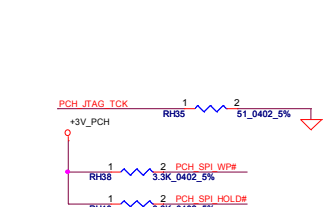
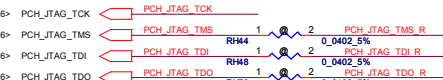
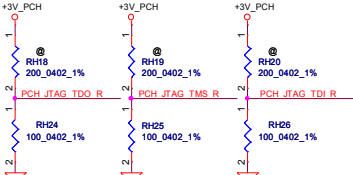
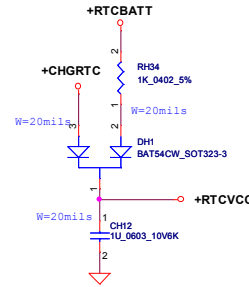


HDA_SDO
ME debug mode, this signal has a weak internal PD
L=>security measures defined in the Flash
Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden

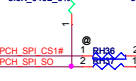


HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platform

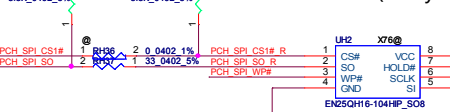
RTC Battery



NEC flash issue.

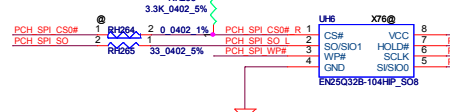


SPI ROM FOR WIN8 (2MByte)



EON
EN25QH16-104HIP_SO8

SPI ROM FOR ME (4MByte)



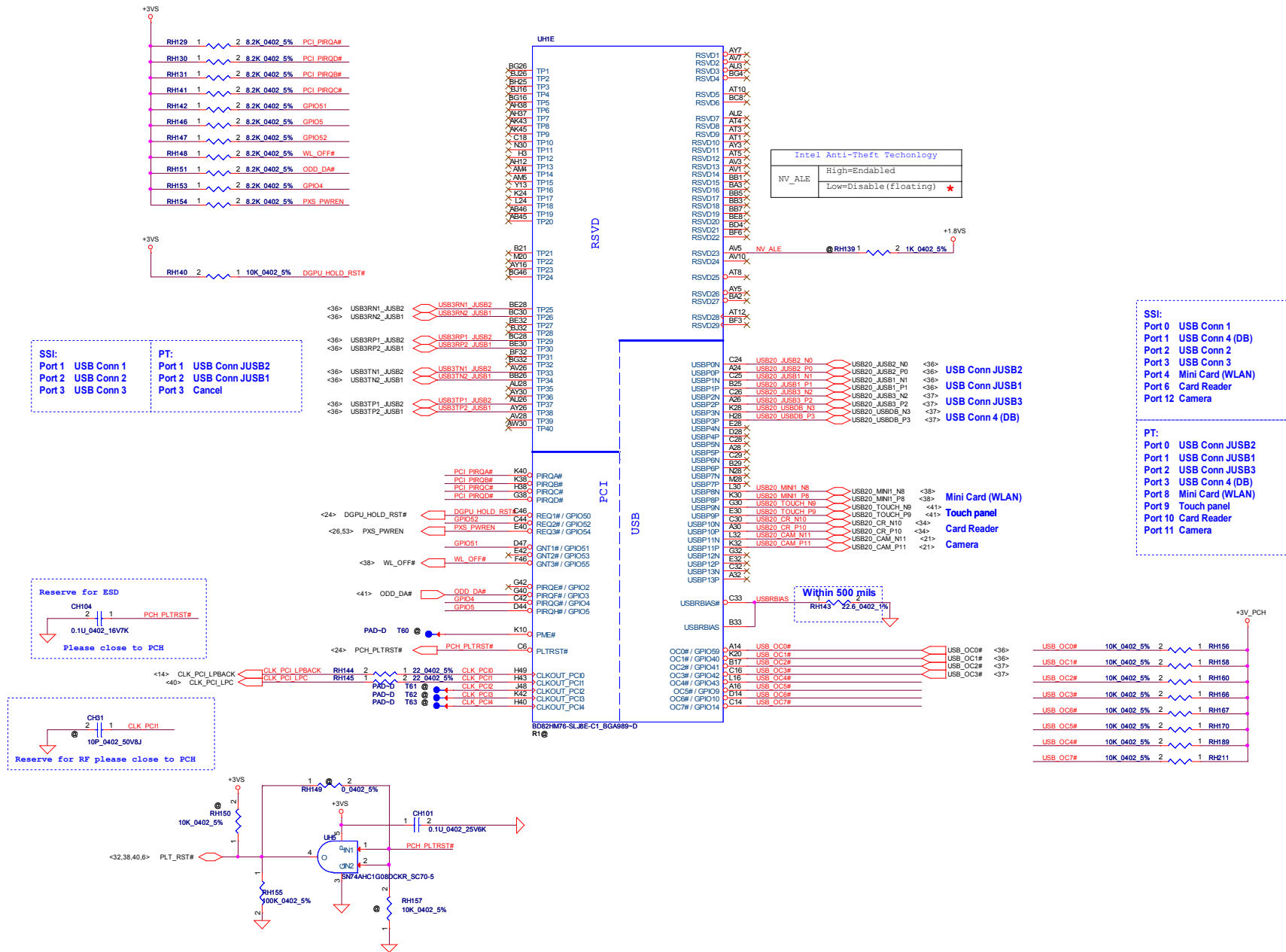
EON
EN25Q32B-104HIP_SO8

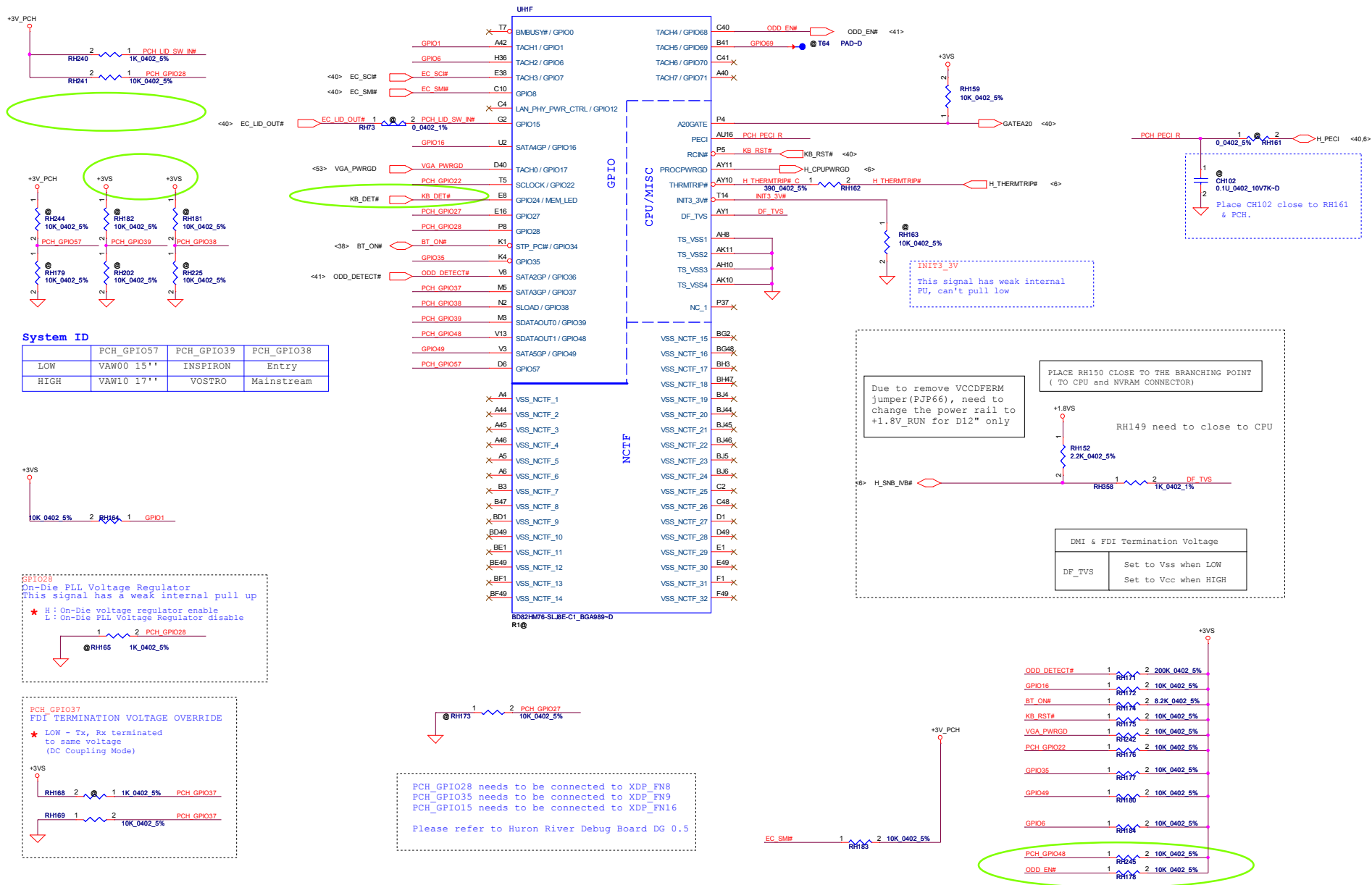


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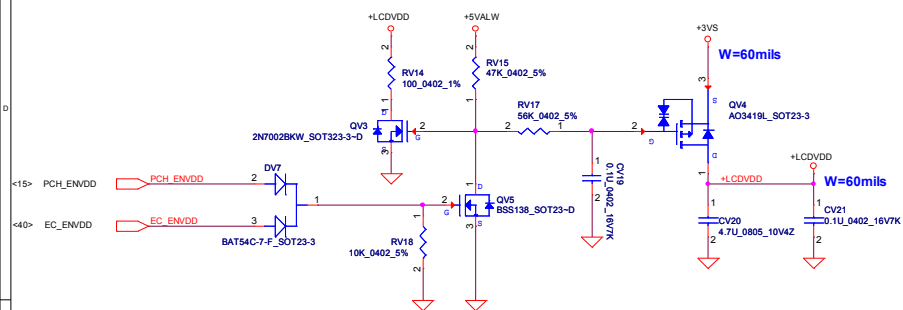


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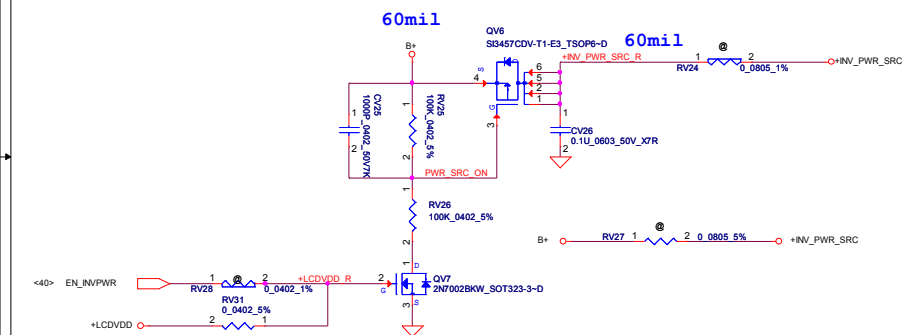




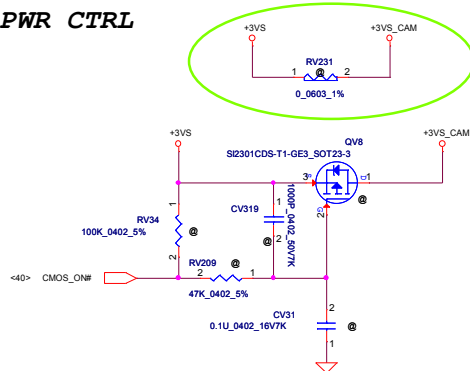
LCD PWR CTRL



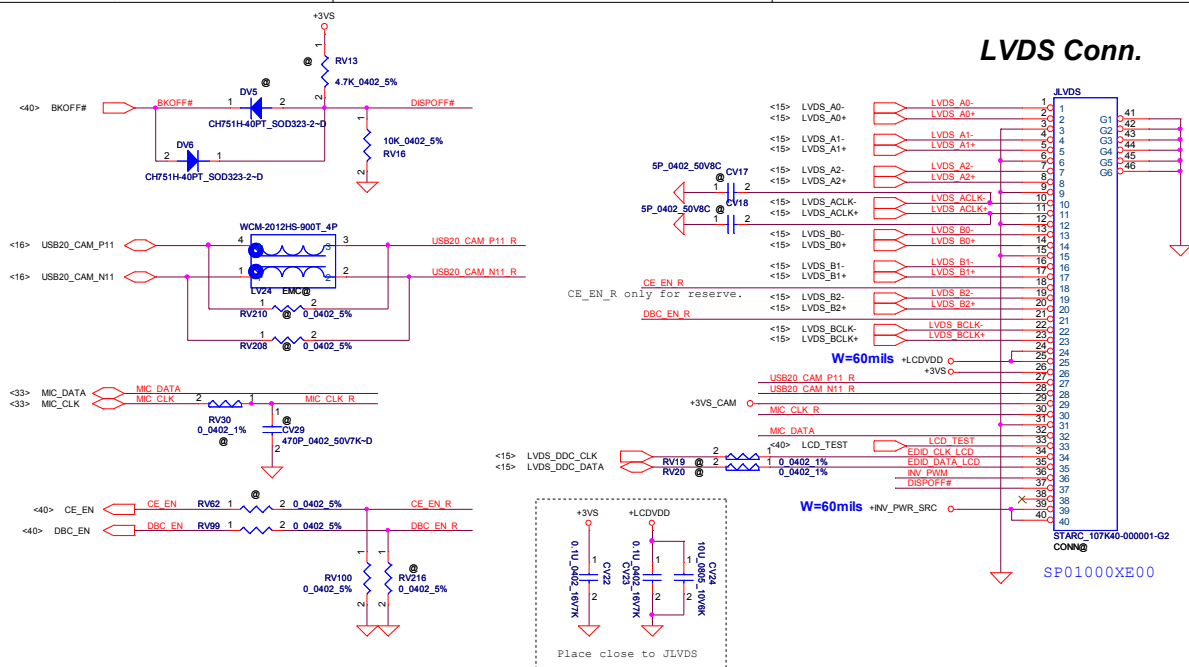
LCD backlight PWR CTRL



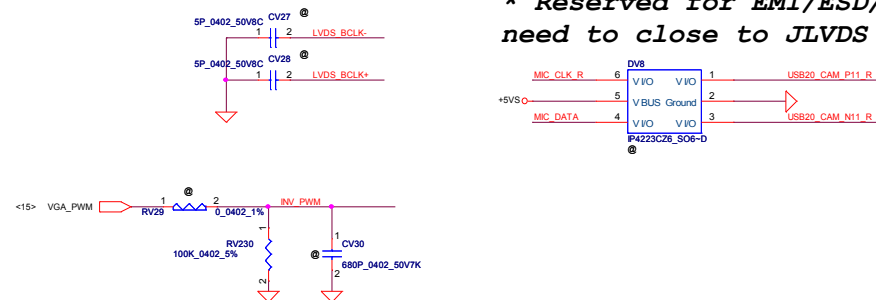
Webcam PWR CTRL



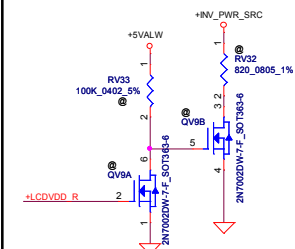
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LVDS Conn.

* Reserved for EMI/ESD/RF
need to close to JLVDS

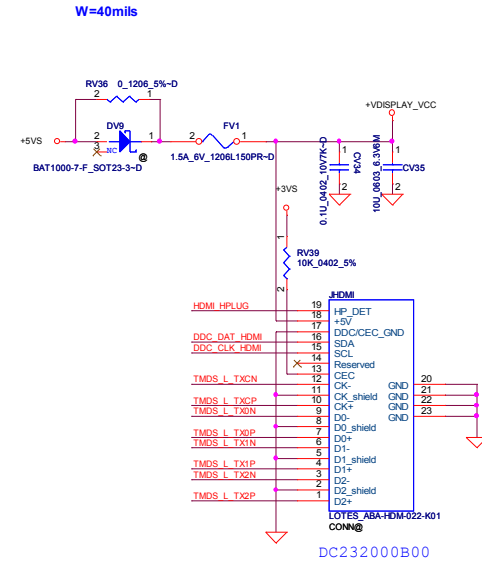
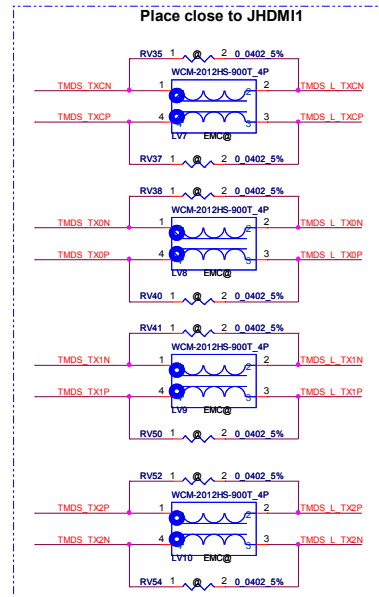
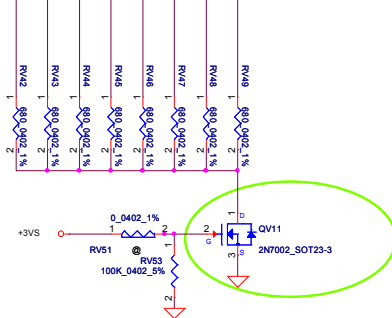


* Reserved for LCD
sequence tuning



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<15>	HDMI_A3N_VGA	CV32	2	1	0.1U_0402_10V7K-D	TMDS_TXCN
<15>	HDMI_A3P_VGA	CV33	2	1	0.1U_0402_10V7K-D	TMDS_TXCP
<15>	HDMI_A0N_VGA	CV36	2	1	0.1U_0402_10V7K-D	TMDS_TXCN
<15>	HDMI_A0P_VGA	CV37	2	1	0.1U_0402_10V7K-D	TMDS_TXCP
<15>	HDMI_A1N_VGA	CV38	2	1	0.1U_0402_10V7K-D	TMDS_TXIN
<15>	HDMI_A1P_VGA	CV39	2	1	0.1U_0402_10V7K-D	TMDS_TXIP
<15>	HDMI_A2N_VGA	CV40	2	1	0.1U_0402_10V7K-D	TMDS_TXCN
<15>	HDMI_A2P_VGA	CV41	2	1	0.1U_0402_10V7K-D	TMDS_TXCP

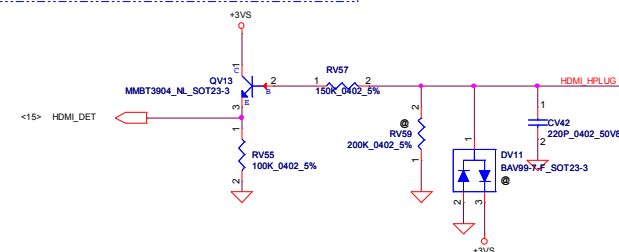
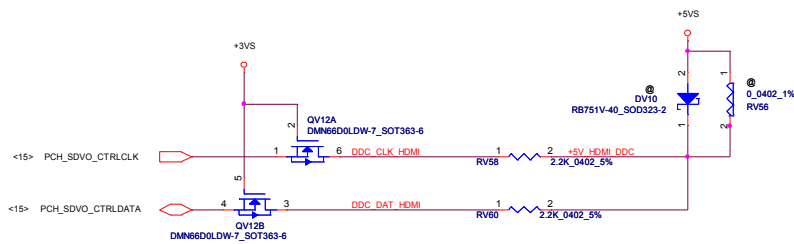


TMDS_TXCN	@ CV358	1	2	100P_0402_50V8J
TMDS_TXCP	@ CV360	1	2	100P_0402_50V8J
TMDS_TXIN	@ CV362	1	2	100P_0402_50V8J
TMDS_TXIP	@ CV363	1	2	100P_0402_50V8J
TMDS_TXIN	@ CV359	1	2	100P_0402_50V8J
TMDS_TXIP	@ CV357	1	2	100P_0402_50V8J
TMDS_TX2N	@ CV361	1	2	100P_0402_50V8J
TMDS_TX2P	@ CV364	1	2	100P_0402_50V8J

20111024 EMI ADD

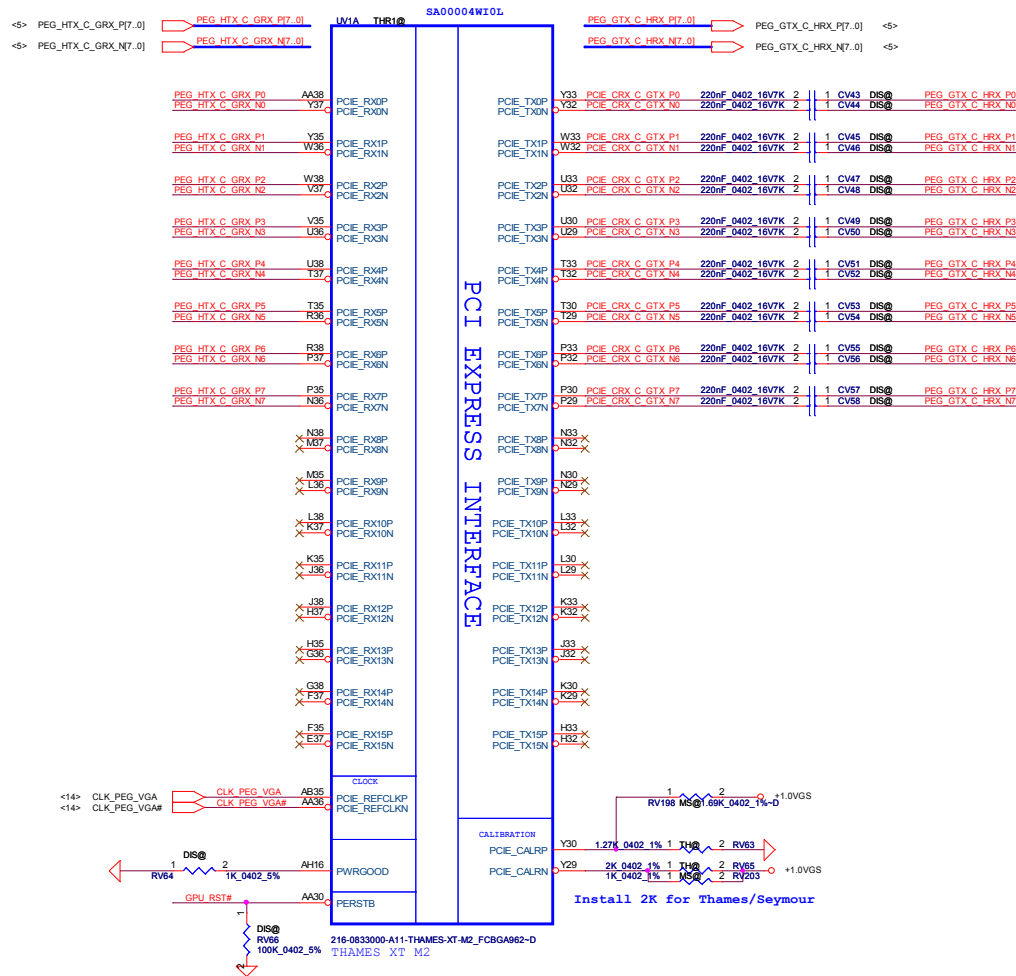
TMDS_L_TXCN	CV349	1	2	3.3P_0402_50V8C-D
TMDS_L_TXCP	CV350	1	2	3.3P_0402_50V8C-D
TMDS_L_TXIN	CV351	1	2	3.3P_0402_50V8C-D
TMDS_L_TXIP	CV352	1	2	3.3P_0402_50V8C-D
TMDS_L_TXIN	CV353	1	2	3.3P_0402_50V8C-D
TMDS_L_TXIP	CV354	1	2	3.3P_0402_50V8C-D
TMDS_L_TX2N	CV355	1	2	3.3P_0402_50V8C-D
TMDS_L_TX2P	CV356	1	2	3.3P_0402_50V8C-D

20110805 EMI ADD

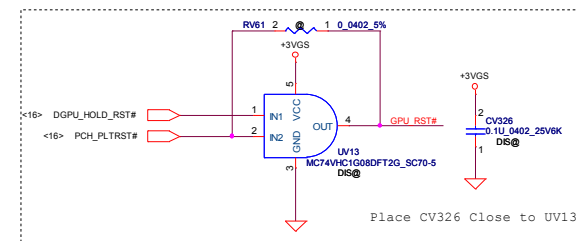
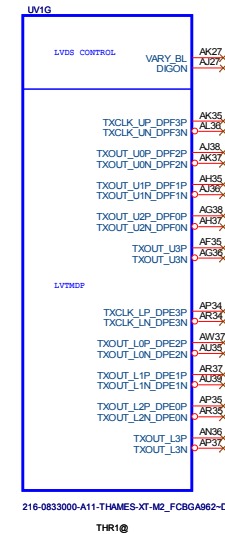


46	ROYALTY HDMI W/LOGO
Part Number	Description
RC000000023M	HDMI W/Logo:RC000000023M

GFX PCIE LANE REVERSAL

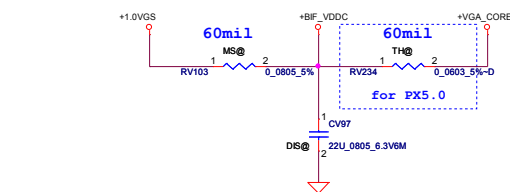


LVDS Interface



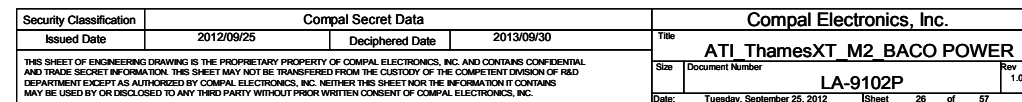


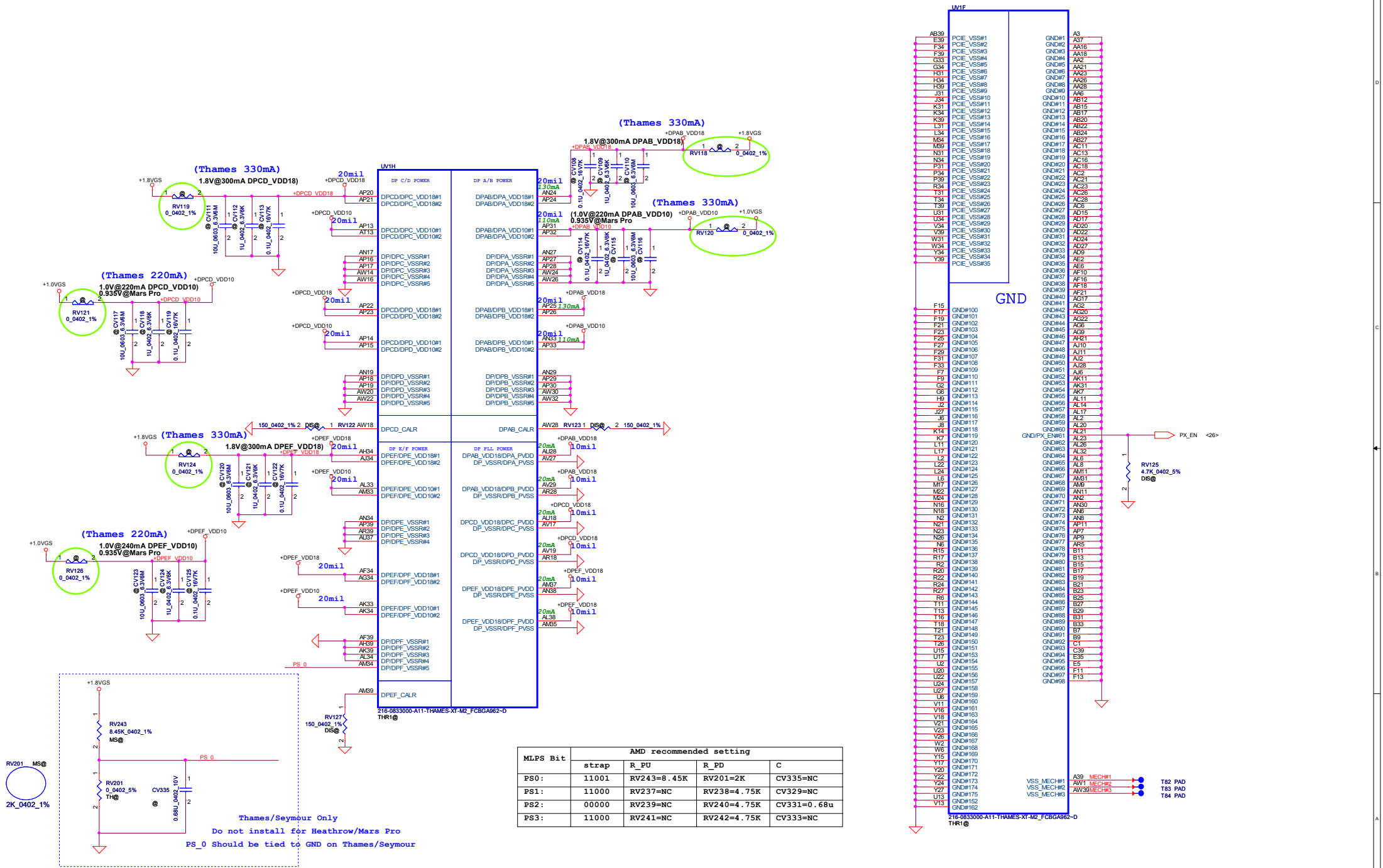
55mA@1.0V, in BACO mode



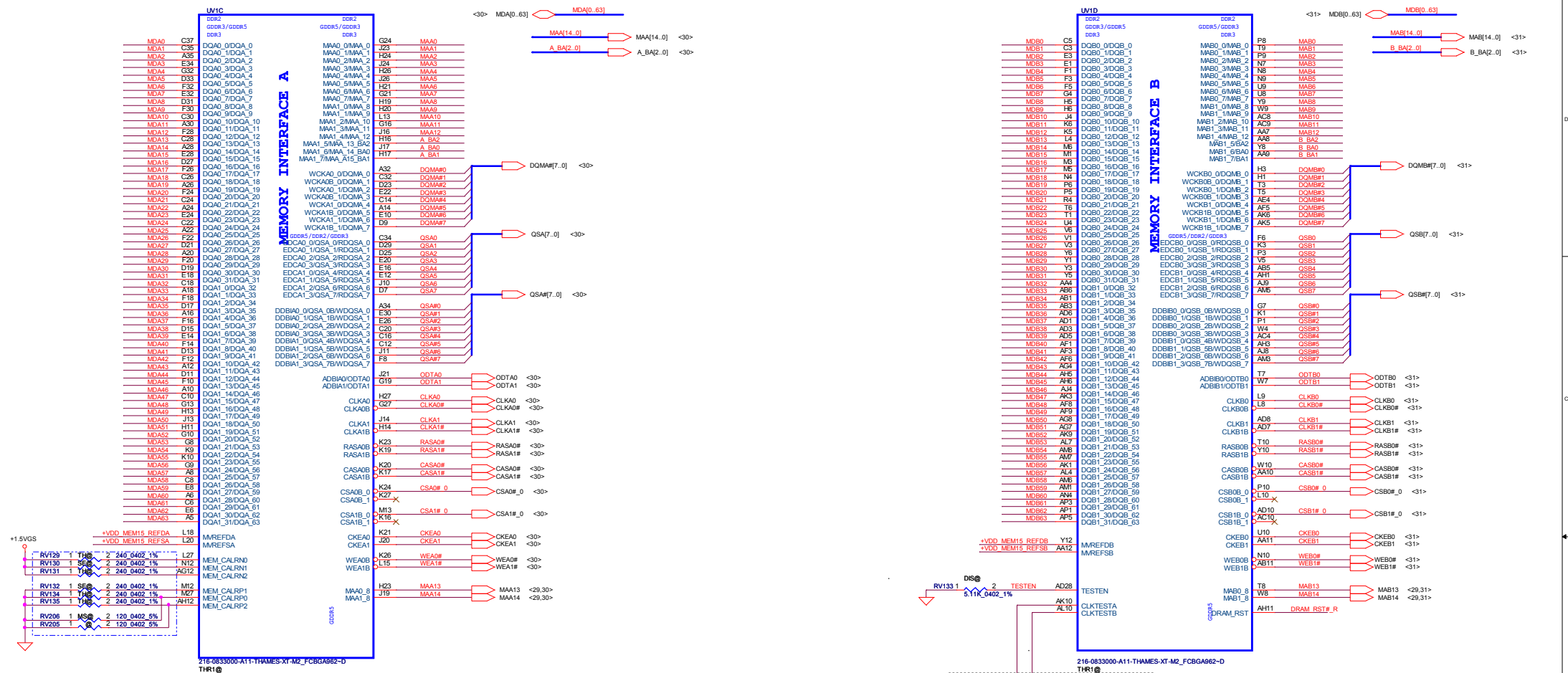
Timing diagram showing the sequence of voltage steps:

- +3VGS
- +VGA_CORE
- +VDDCI
- +1.5VGS
- +1.0VGS
- +1.8VGS
- <20ms





MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

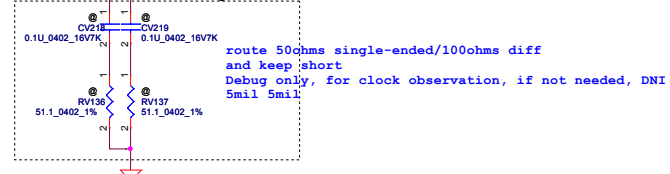
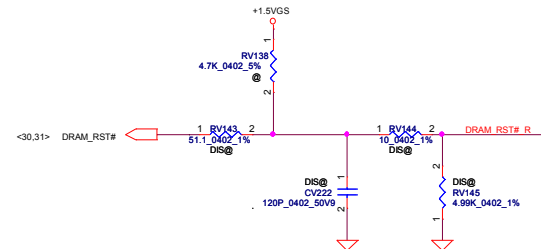


Co-lay Thames/Seymour/Mars Pro

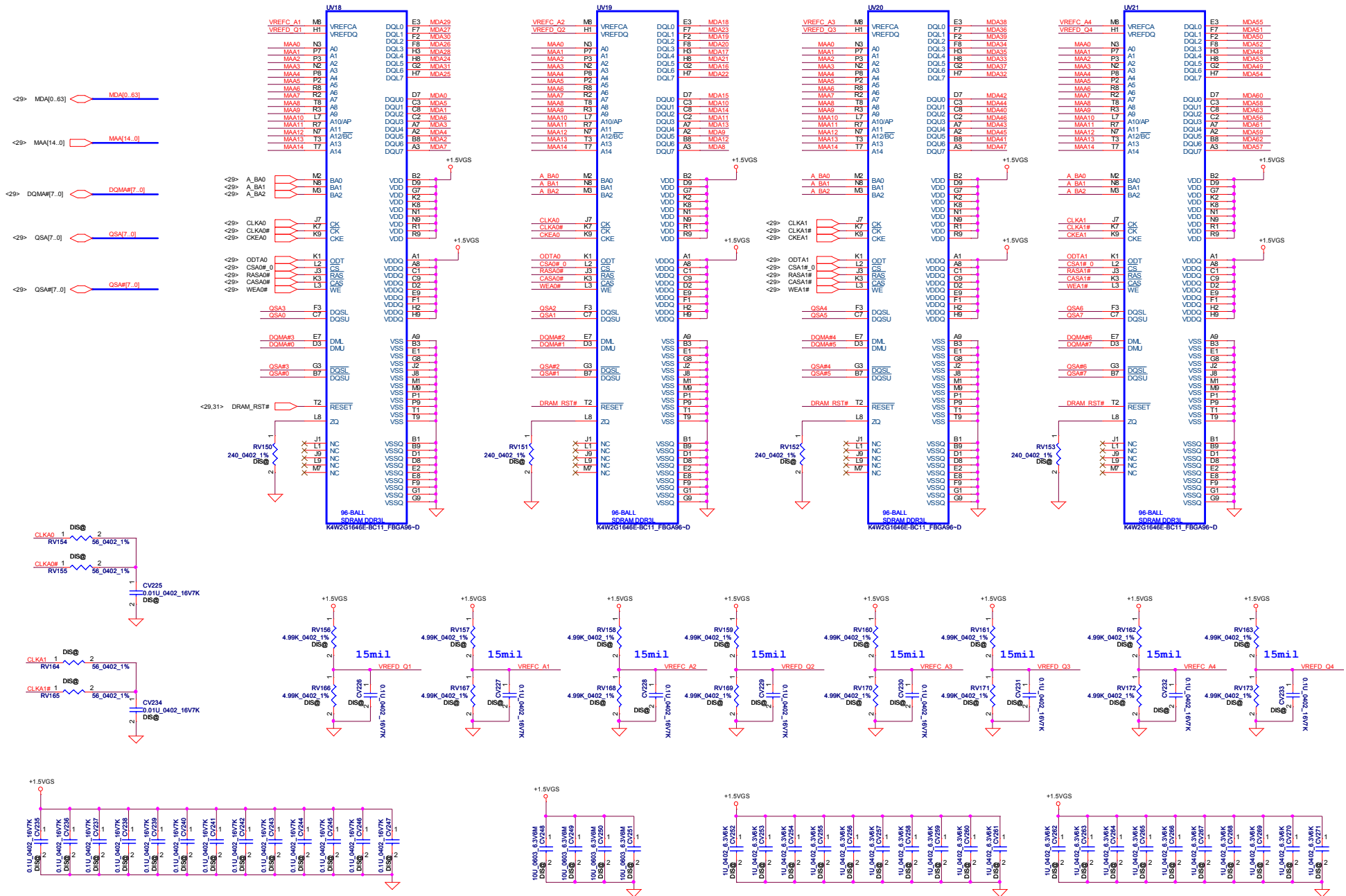
	Thames M2	Seymour M2	Mars Pro
RV129	TH@	@	@
RV130	@	SE@	@
RV131	TH@	@	@
RV132	@	SE@	@
RV134	TH@	@	@
RV135	TH@	@	@
RV206	@	@	MS@
RV205	@	@	@

This basic topology should be used for DRAM RST# for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and I Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec.

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

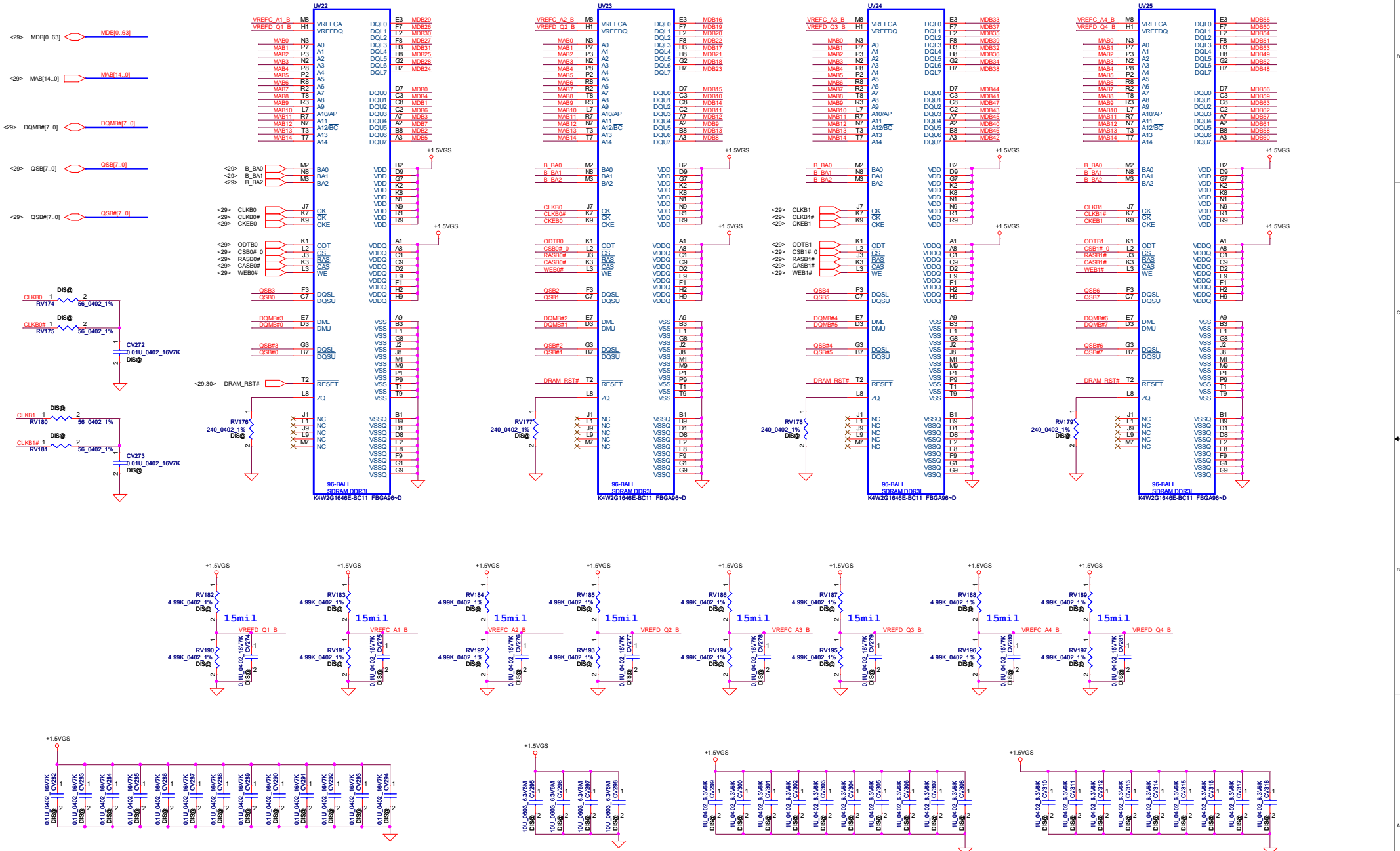


CHANNEL A: 256MB/512MB DDR3



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2012/09/25	Deciphered Date	2013/09/30	Title	ATI ThamesXT M2 VRAM A	
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				LA-9102P		1.0
Date:		Tuesday, September 25, 2012		ISheet	30	of 57

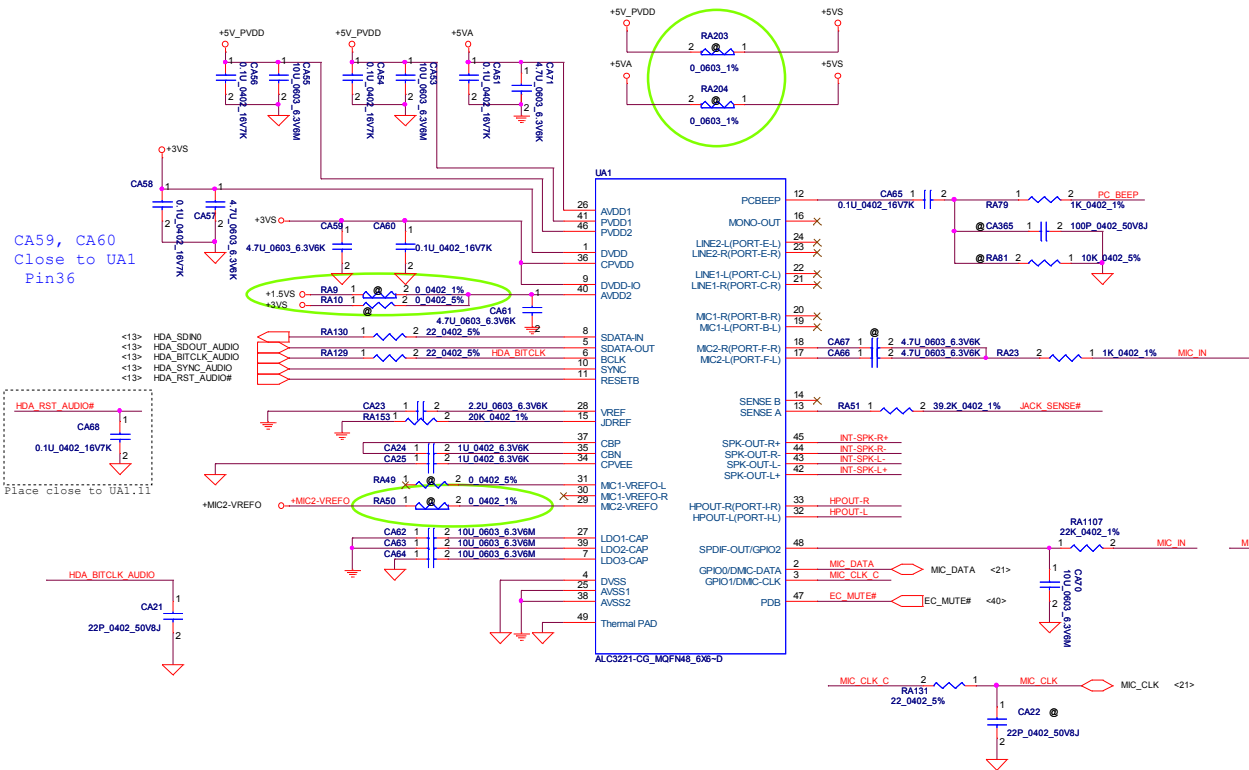
CHANNEL B: 256MB/512MB DDR3



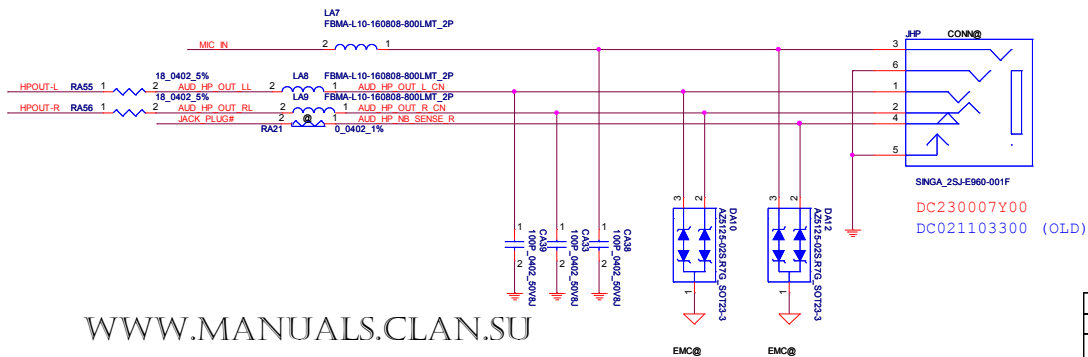
CA59, CA60
Close to UA1
Pin36

HDA_RST_AUDIO#
0.1u_0402_16V7K
Place close to UA111

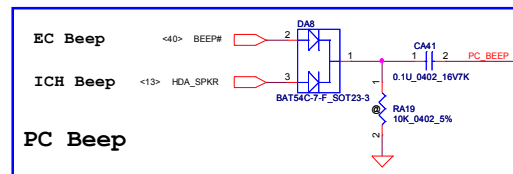
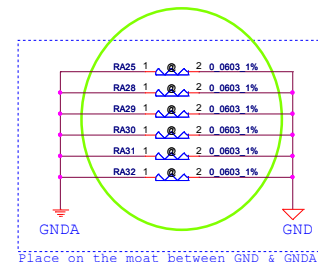
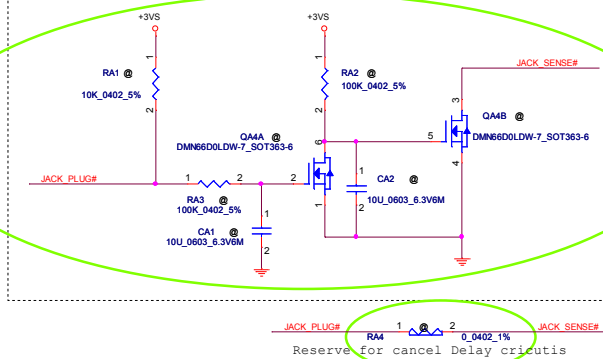
HDA_BITCLK_AUDIO
CA21
22P_0402_50V8J



iPhone type Combo Jack

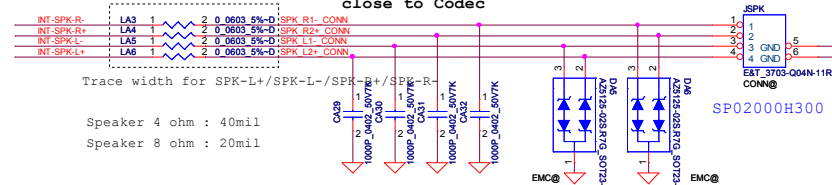


JACK_PLUG Delay circuit

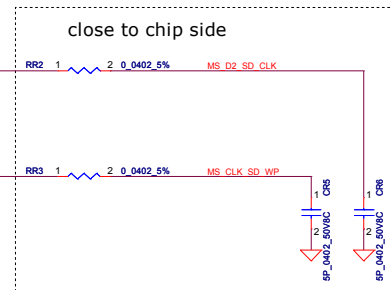
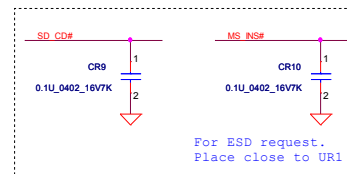
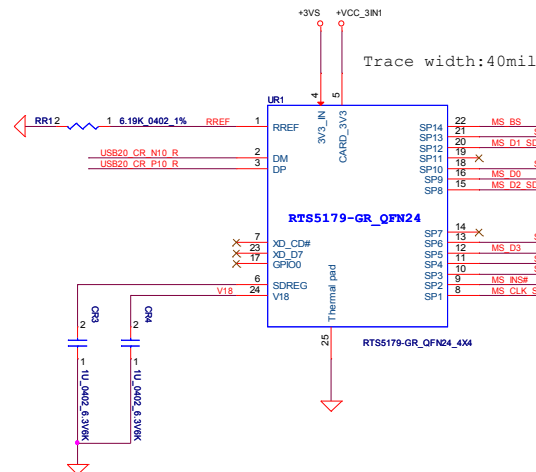
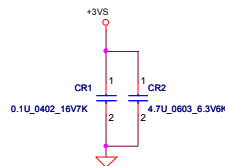
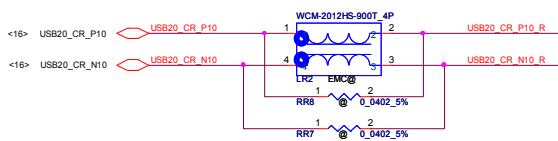


Close to UA1
Pin11,13,14,16

close to Codec

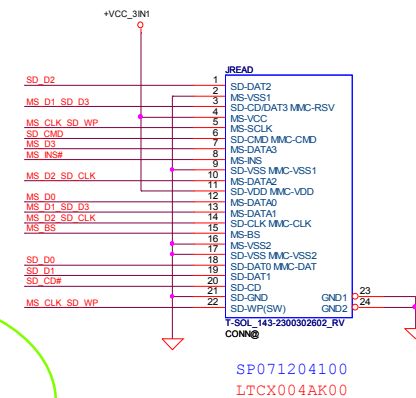
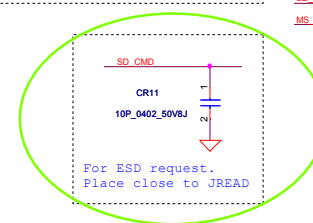
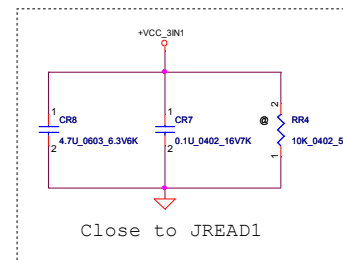


Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



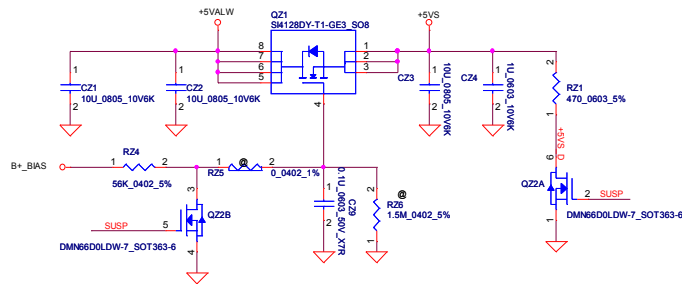
拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

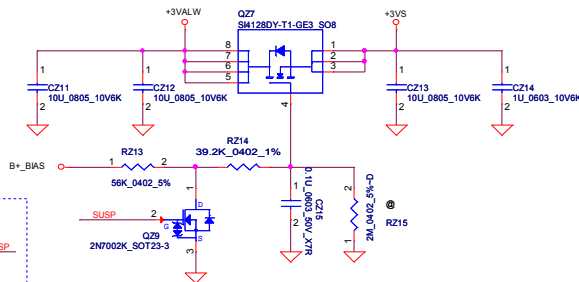


SP071204100
LTCX004AK00

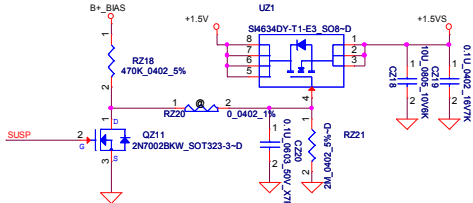
+5VALW to +5VS



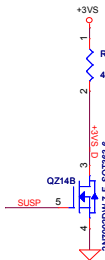
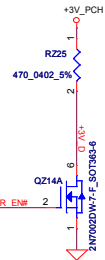
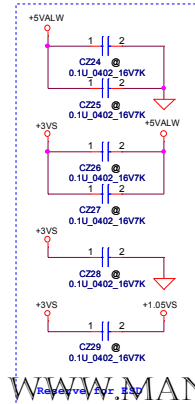
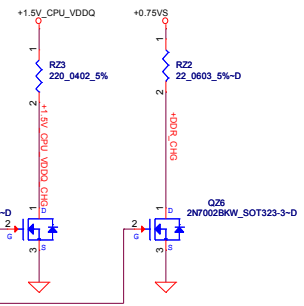
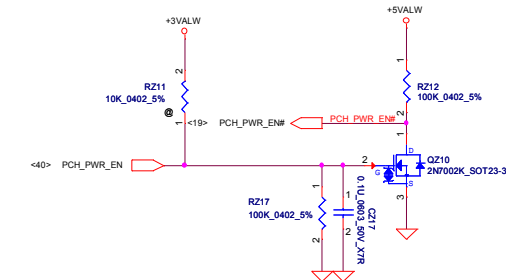
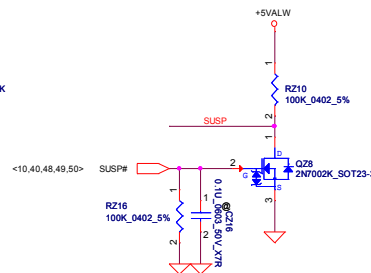
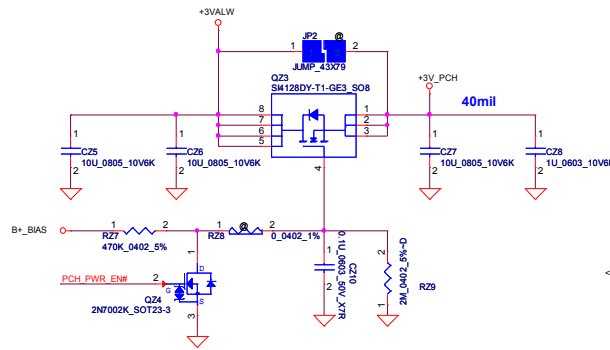
+3VALW to +3VS

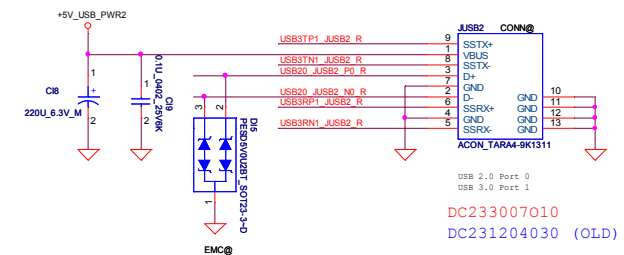
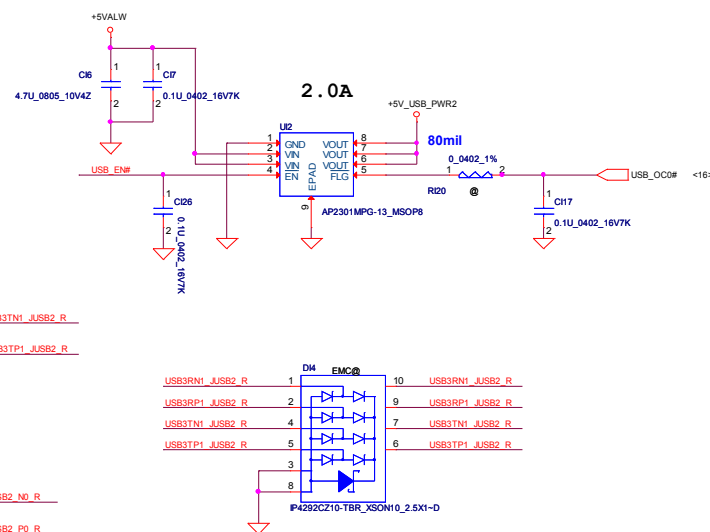
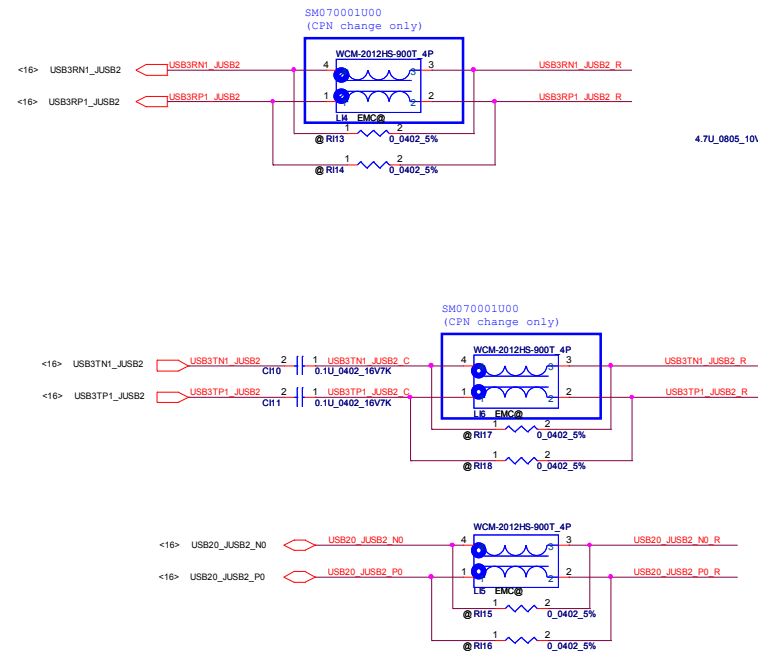
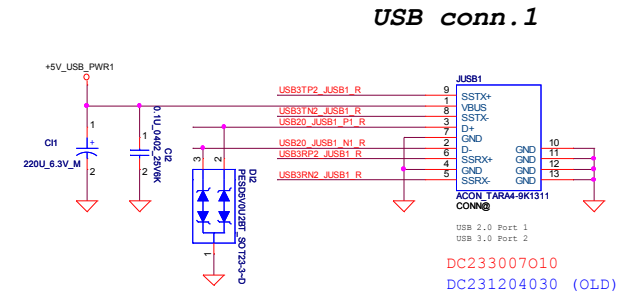
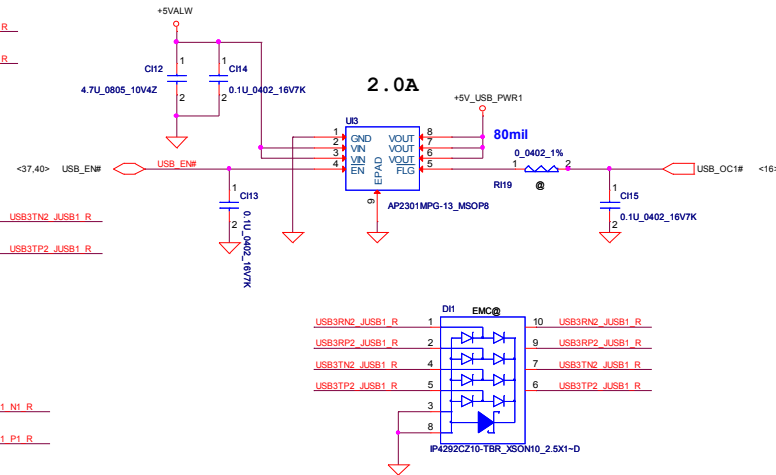
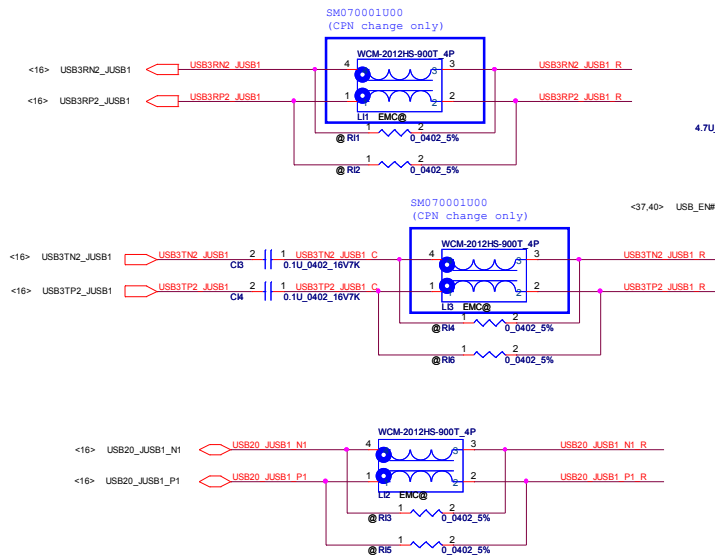


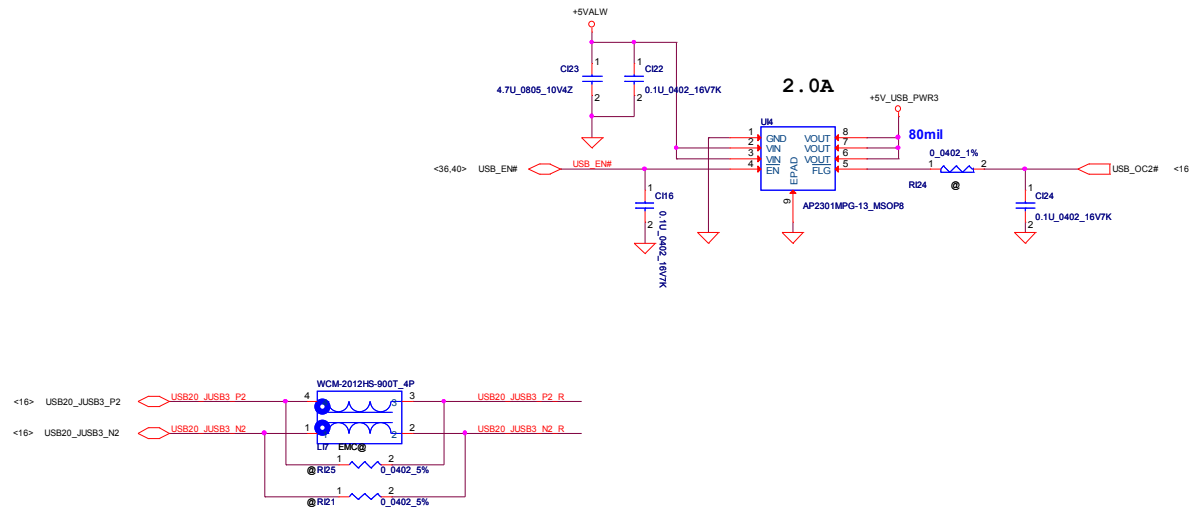
+1.5V To +1.5VS



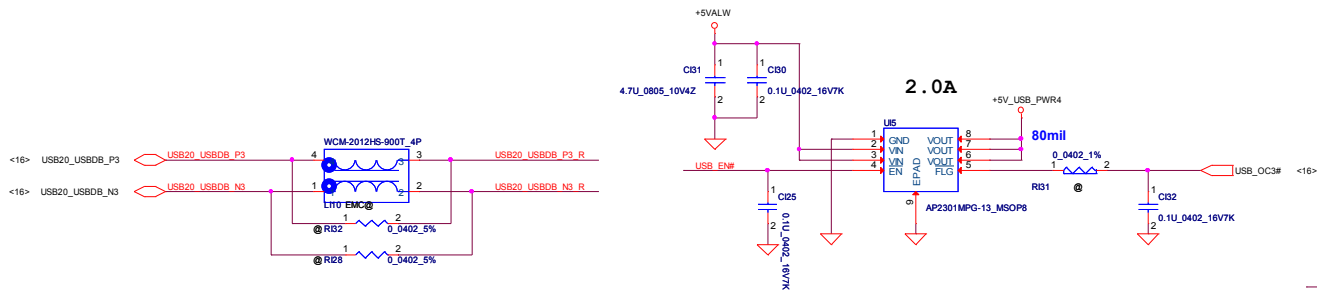
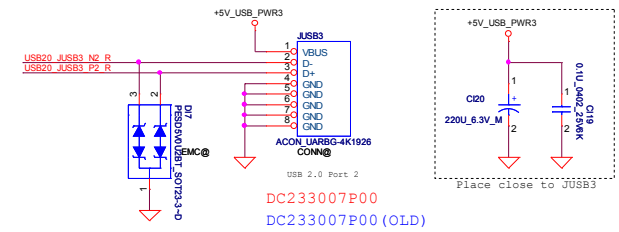
+3VALW to +3V_PCH



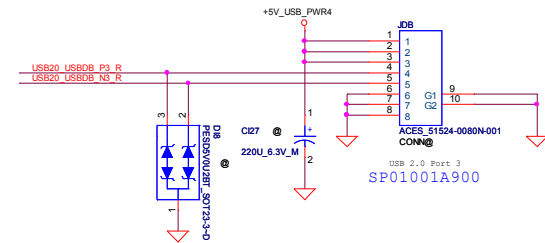




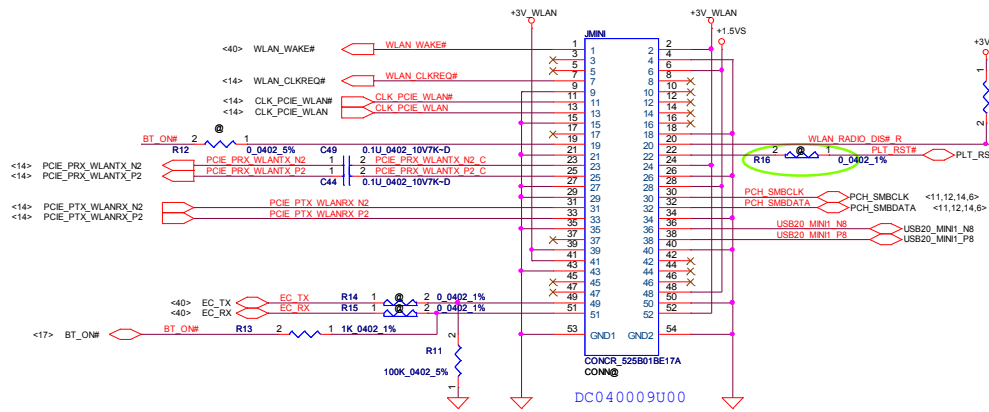
USB conn.3



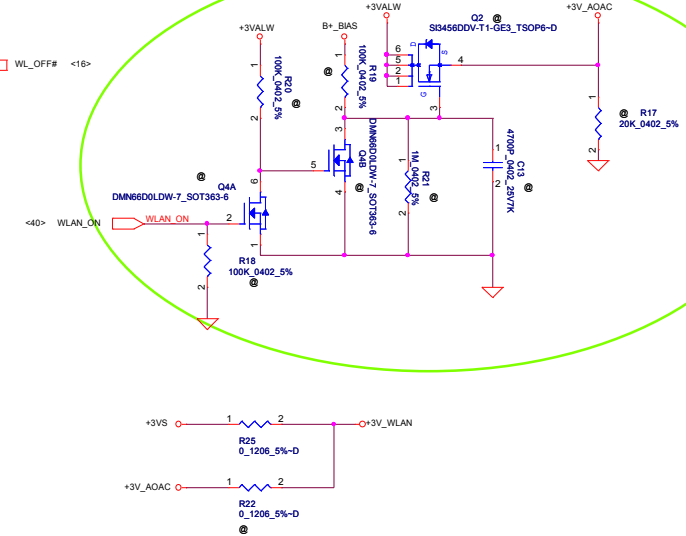
USB conn.4



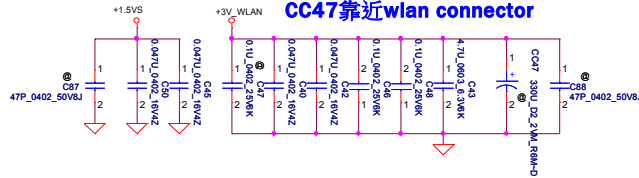
Mini WLAN/WIMAX H=6.7



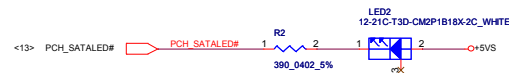
Power Control for Mini card



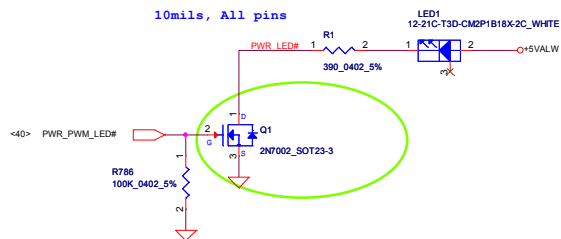
CC47靠近wlan connector



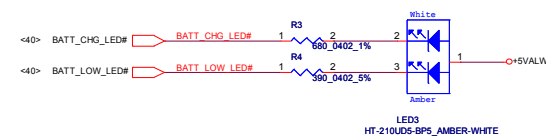
HDD LED



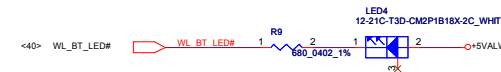
Power LED



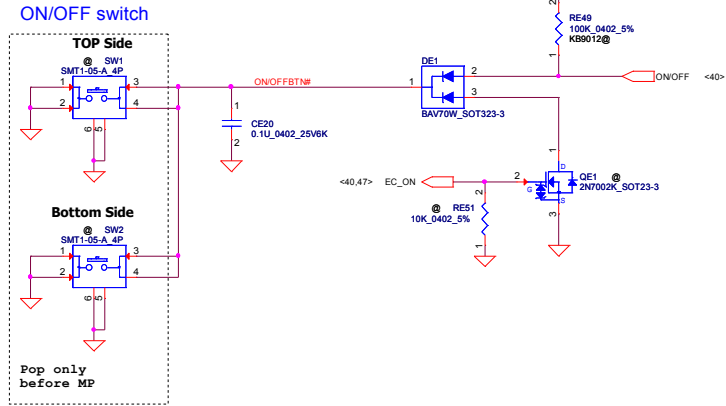
Battery LED



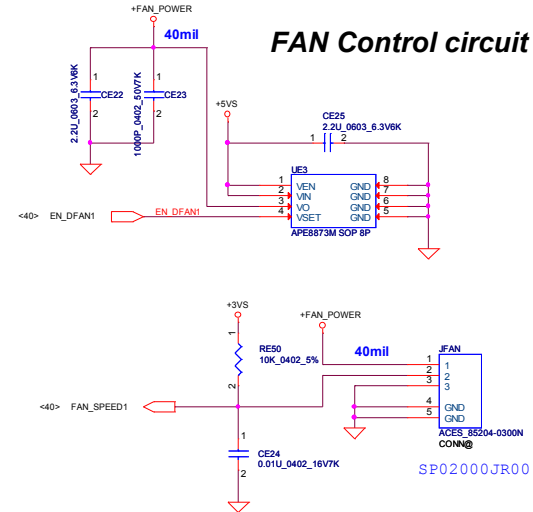
Wireless LED



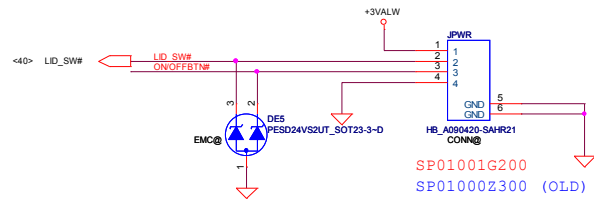
Power ON Circuit



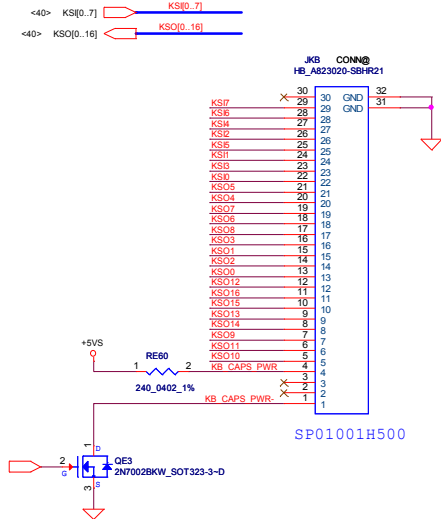
FAN Control circuit



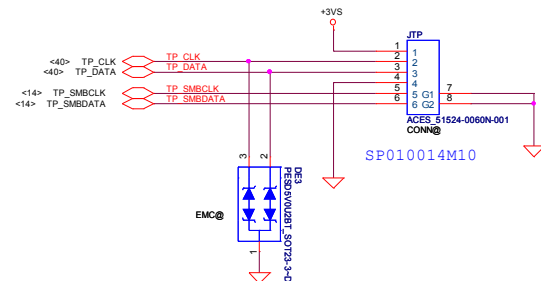
POWER/B

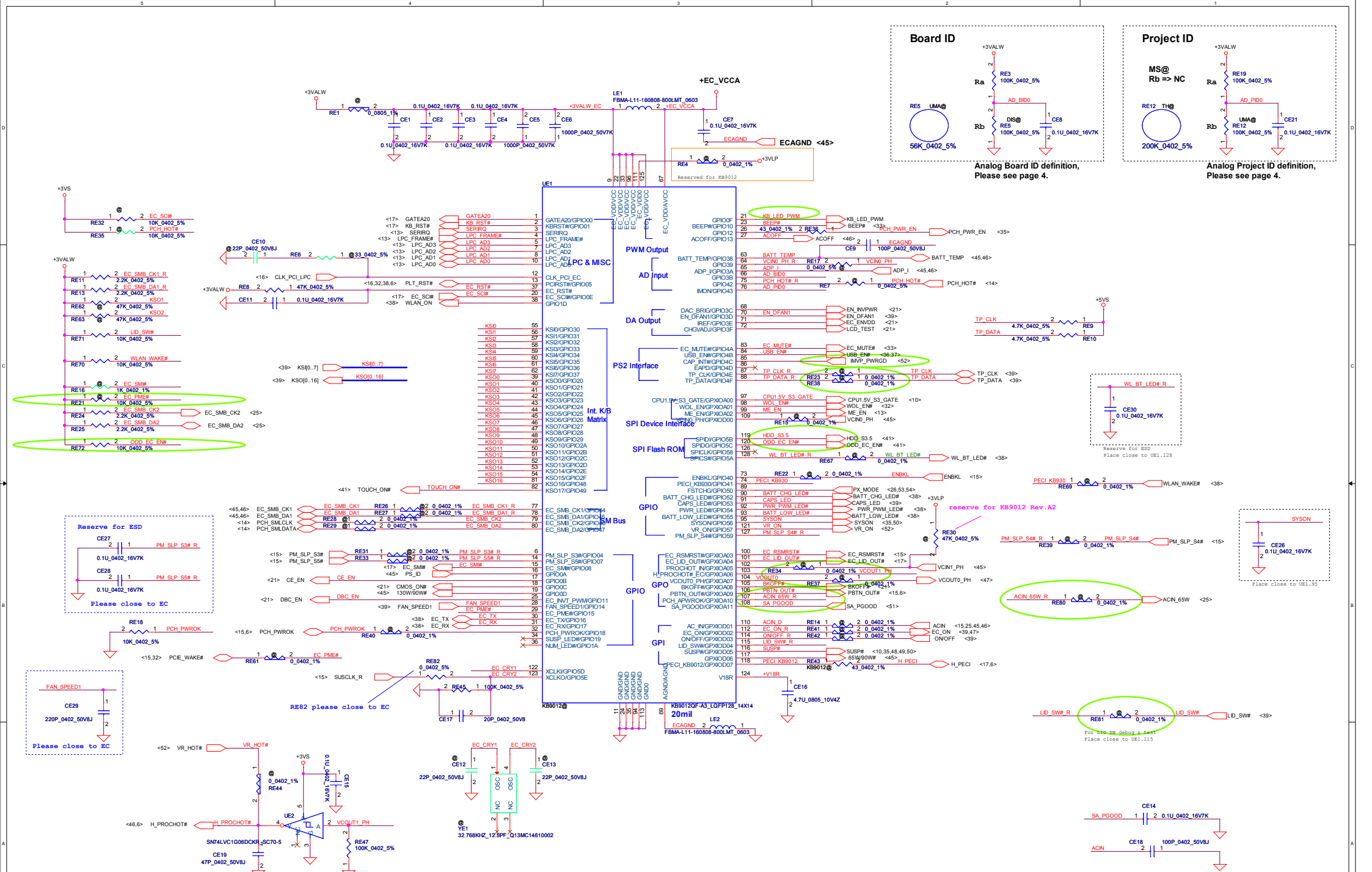


INT_KBD Conn.



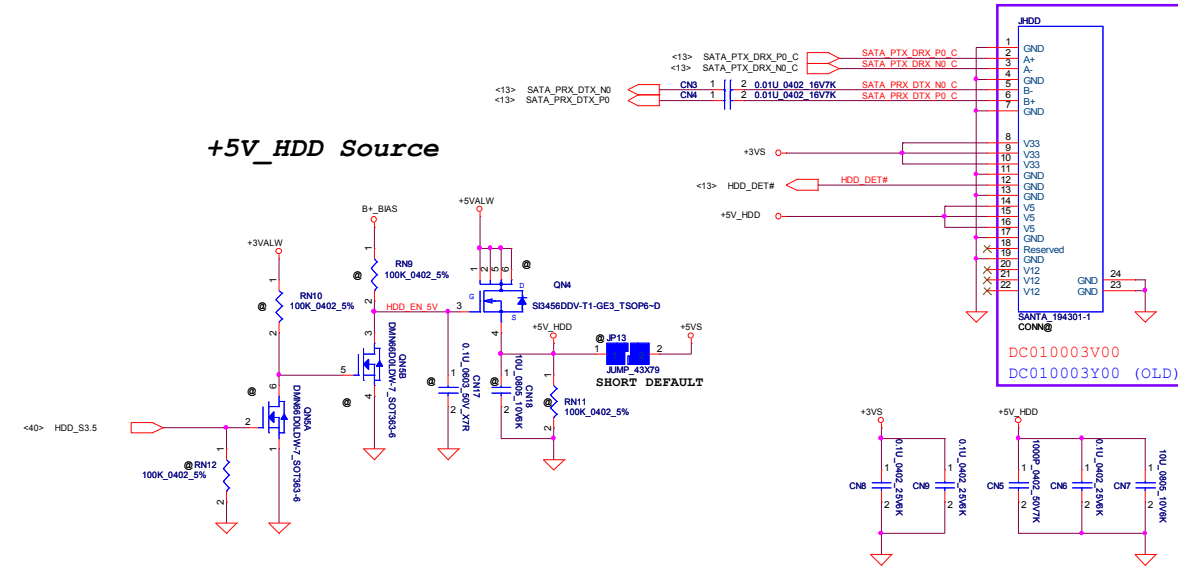
Touch pad



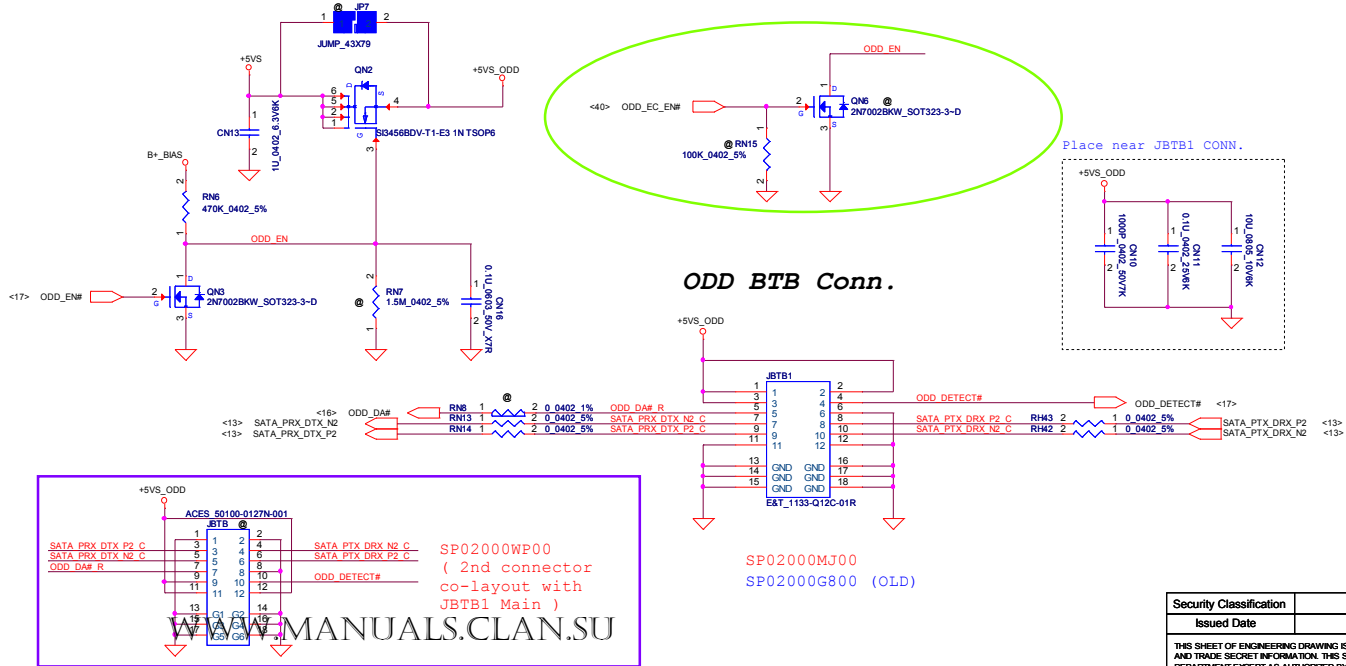


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Issued Date	2012/09/25	Deciphered Date	2013/09/30	Compal Electronics, Inc.	
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				LA-9102P	Rev 1.0
				Date: Tuesday, September 25, 2012	Sheet 40 of 57

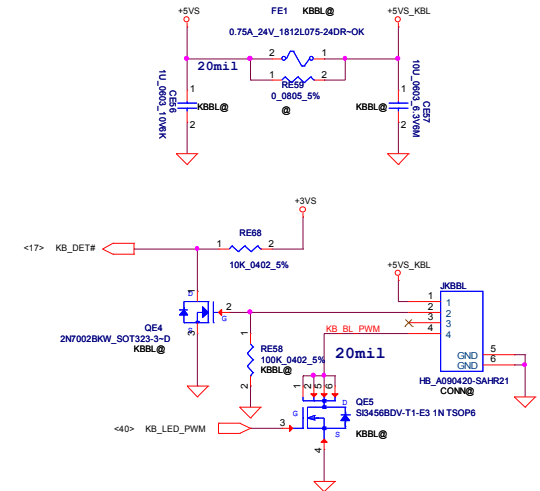
SATA HDD Conn.



ODD Power Control

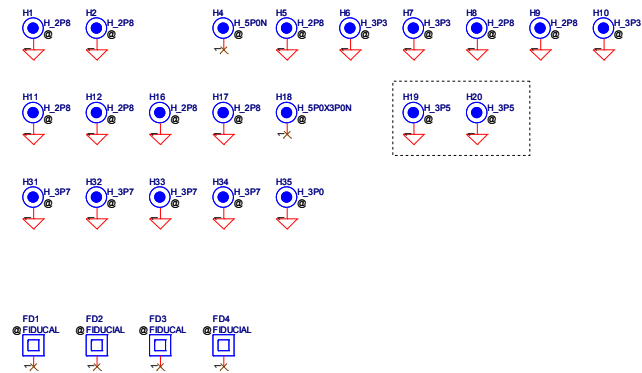


* *Key Board Back Light*



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Date:				Tuesday, September 25, 2012	Sheet	41 of 57

Screw Hole



Version Change List (P. I. R. List)

Page 1

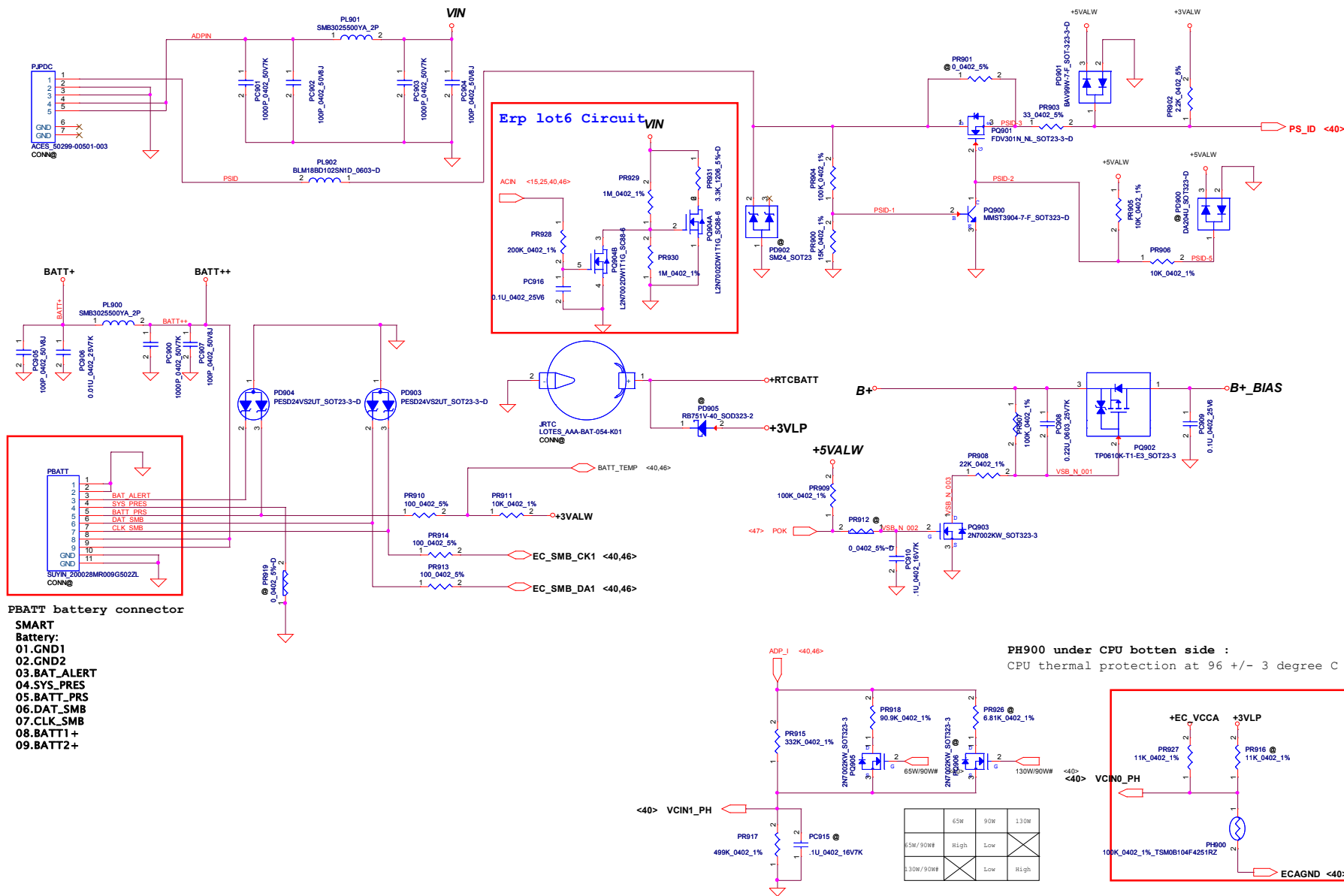
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21,39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
2	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
3	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add AUDIO JACK PLUG delay circuit. Separate NET JACK_PLUG to => JACK_SENSE# & => JACK_PLUG#	0.2
4	16,21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
5	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RES from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)	0.2
6	21,39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET "TOUCH_ON#" from JTOUCH to UEI.82(KB9012) for TOUCH_SCREEN_PANEL power control	0.2
7	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1,QA1,QA2,QA3,RA24,RA26,RA60,RA62,RA68,RA109,CA72,CA73	0.2
8	15,16, 39,41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104,C223,CH105,CE27,CE29	0.2
9	14	Green CLK	2012/05/30	HW	For Green CLK test	Change WH31,RH41,RV232 0ohm form "GCLK#" to "g" for break the clock signal to device	0.2
10	10,26,41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 330K/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, RZ18 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0403	0.2
11	41	DC/DC	2012/05/31	HW	For power sequence trunning	Change RZ15 to DE-POP	0.2
12	06,15,16, 39,41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "g" to POP	0.2
13	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21,RL30 from "g" to "GCLK#"	0.2
14	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change RZ4,RZ13 from 470K/0402 56K/0403	0.2
15	35,41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
16	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move CH9,CH10 from Page.13 to Page.41	0.2
17	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.2
18	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "g"	0.2
19	21,35, 39,40,41	Circuit adjust	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.2
20	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.2
21	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75,RV76,RV81 from "DIS#" to "TH#"	0.2
22	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS#" to "g"	0.2
23	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "g"	0.2
24	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "g" to POP	0.2
25	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VLP) & UG1.9(+3VALW) connect to +LAN_IO 2. Add R787 connect from +RTCBATT to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788 0ohm/0402 from +RTCVCC to UG1 for GCLK & DH1 select	0.2
26	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.2
27	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.2
28	41	Connector	2012/07/10	ME	For ME request	Change JBTB1 footprint from SP02000G800 (OLD) to SP02000MJ00	0.2
29	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44,RH46,RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_TDO_R for break signal trace	0.2
30	40	PCH	2012/07/11	ESD	Follow ESD team request	1.Change NET_NAME "N591107274" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.2
31	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVDS.18	0.2
32	32	Connector	2012/07/12	ME	For ME request	Change JLAN CPN from "DC234004V00" to "SP011207090"	0.2
33	40	FAN	2012/07/16	HW	For FAN_SPEED1 noise issue	Change CE29 from "g" to POP	0.2
34	14	Touch PAD	2012/07/17	SED	Change Touch PAD SMBUS port for SMBUS issue	Change Touch PAD SMBUS port for SMB0 to SMB	0.3
35	32	GREEN CLK	2012/07/19	HW	Follow Silego FAE request	Change RL21 from 510 ohm to 0 ohm/0402	0.3
36	41	Touch Screen	2012/08/07	SED	Follow SED team request change JTOUCH USB signal conatct.	Change JTOUCH Pin define.	0.3
37	34	Card Reader	2012/08/14	ESD	Follow ESD team request	Reserve CR11 100p/0402 close to JREAD	0.3
38	23	GREEN CLK	2012/08/16	HW	Fixed GCLK output abnormal issue	Change UG1.2(UG1/VDD) from +LAN_IO to+3VALW	0.3
39	33	CODEC	2012/08/16	HW	The issue already fixed by new CODEC.	Remove delay circuit and POP RA4	0.3

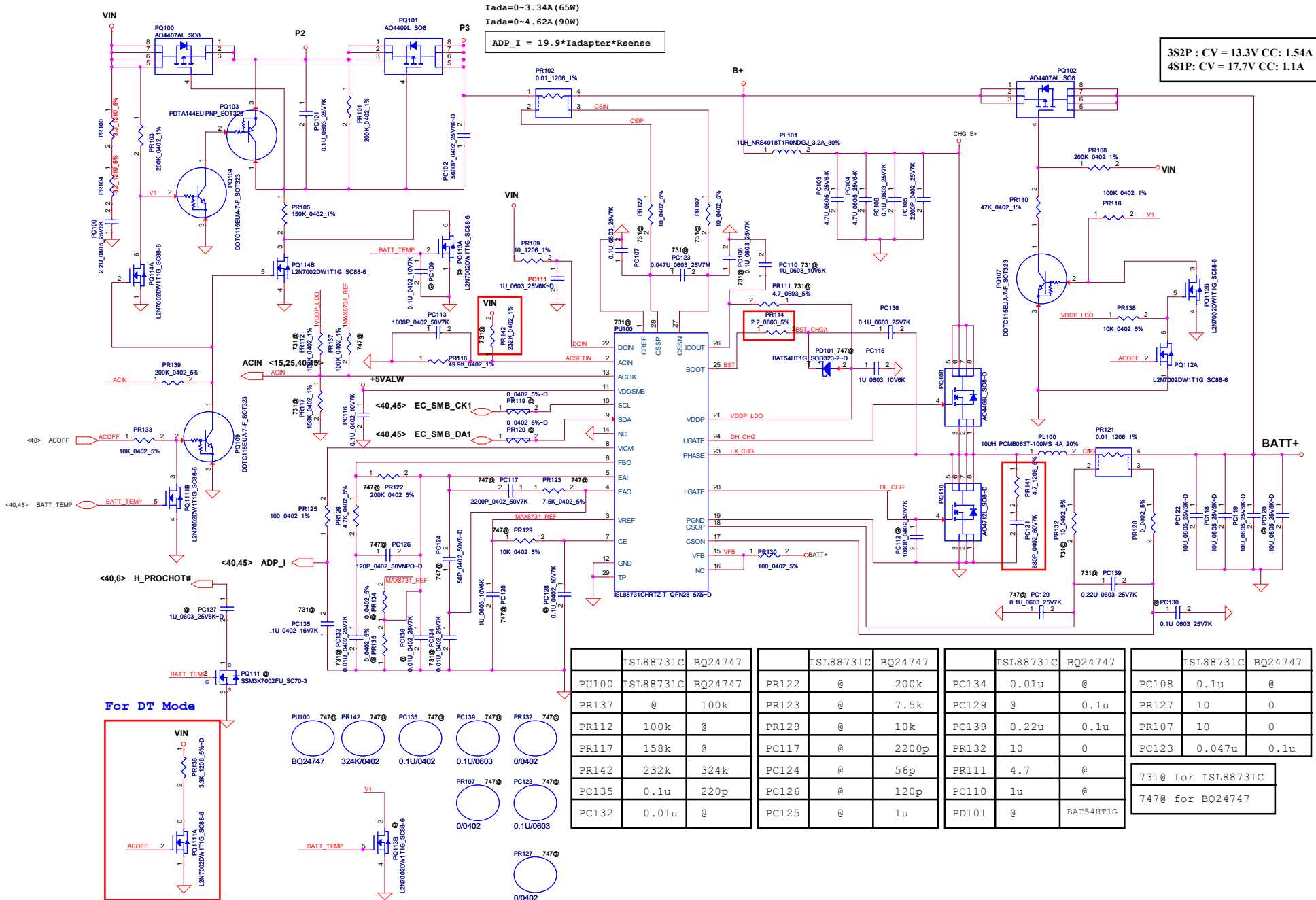
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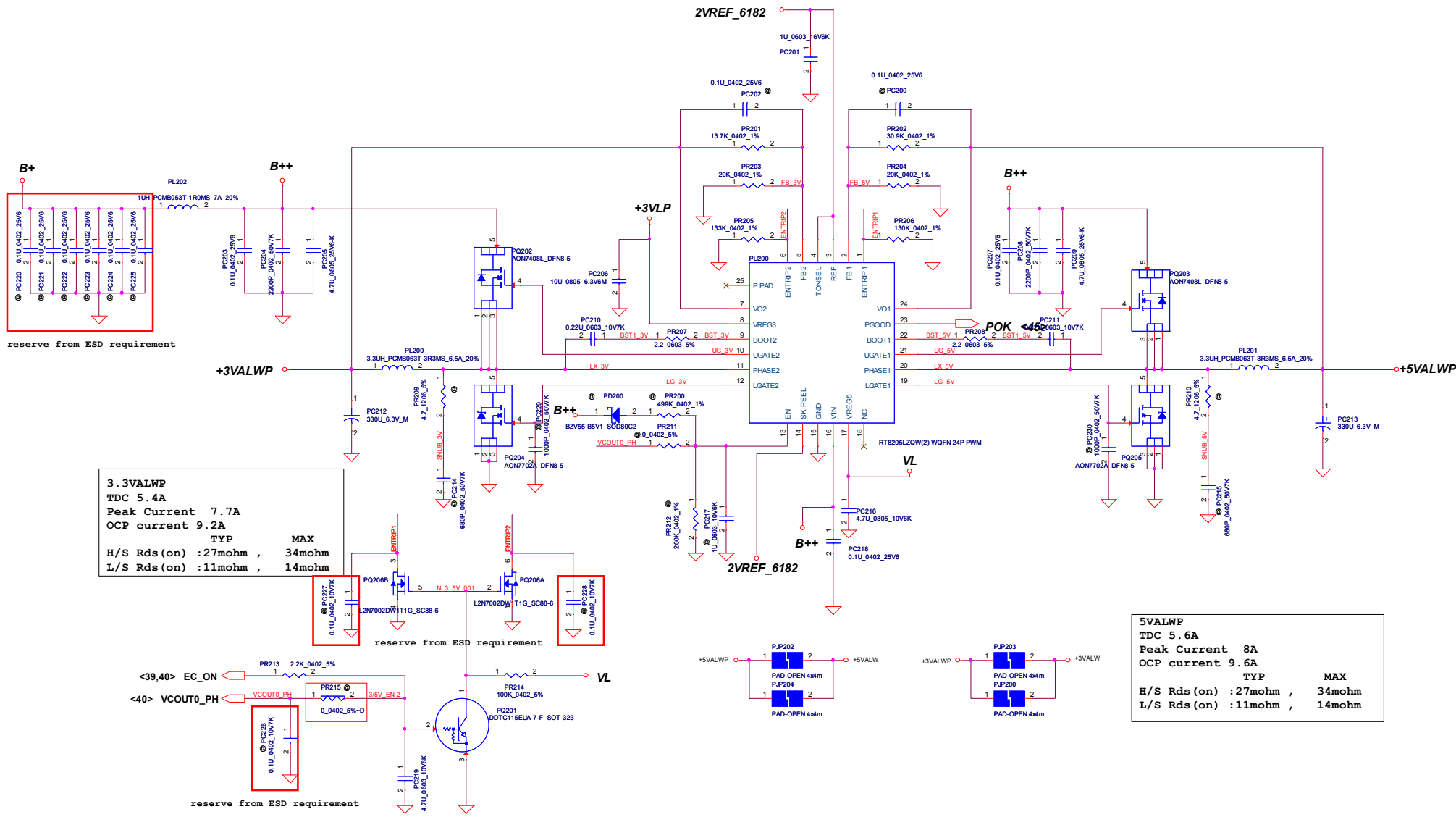
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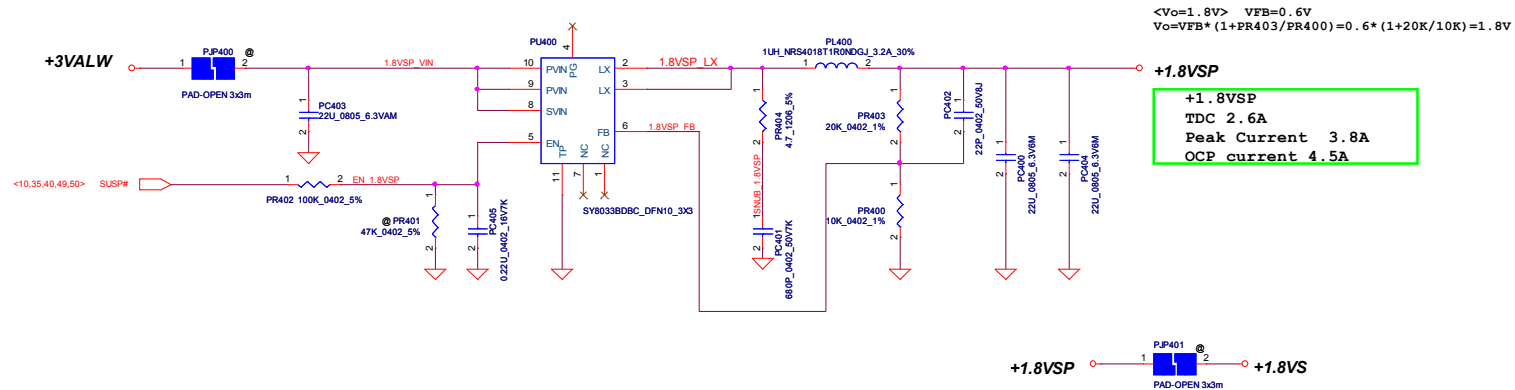
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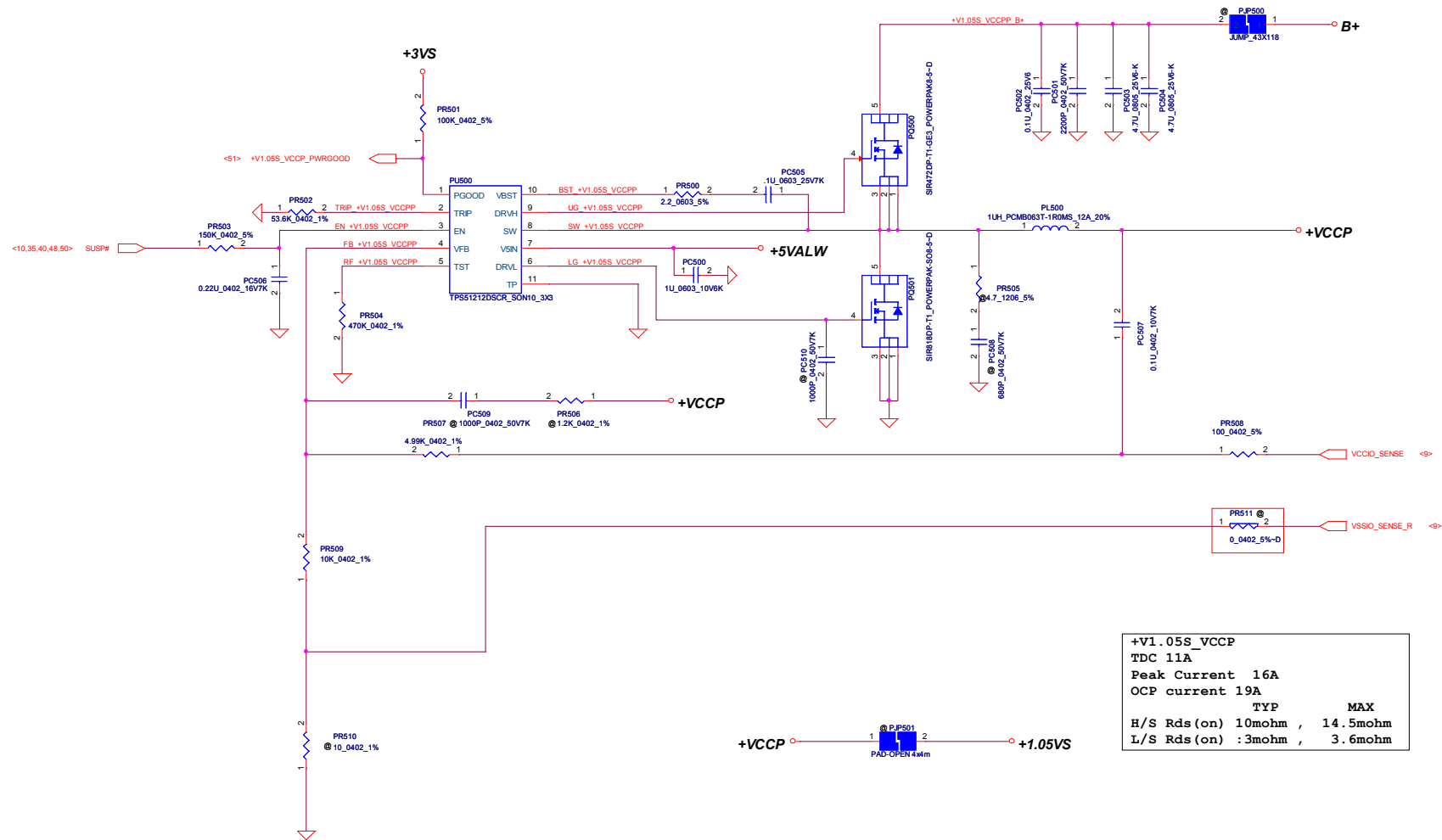
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1.5VP
TDC 6A
Peak Current 8A
OCP current 10A

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

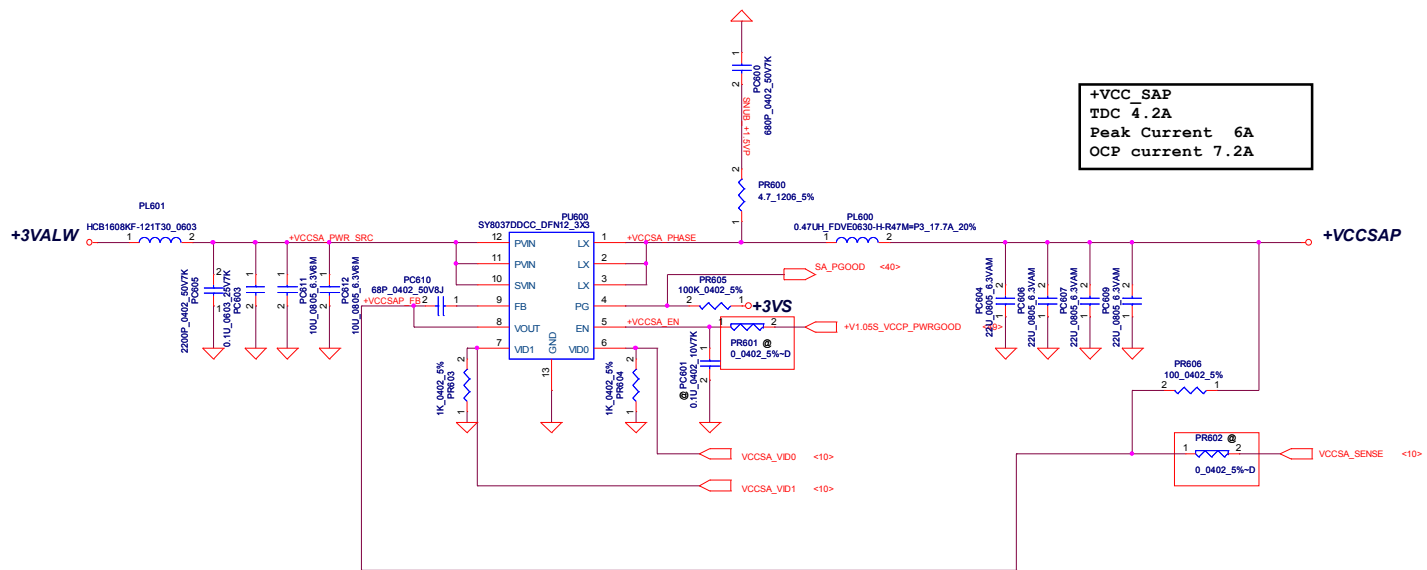
+1.5VGPU
TDC 4.2A
Peak Current 6A
OCP current 7.2A

<10,35,40,48,49> SUSP#

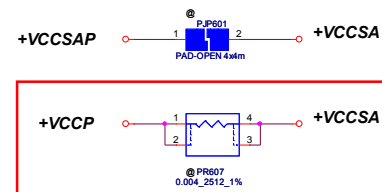
<35,40> SYSON

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

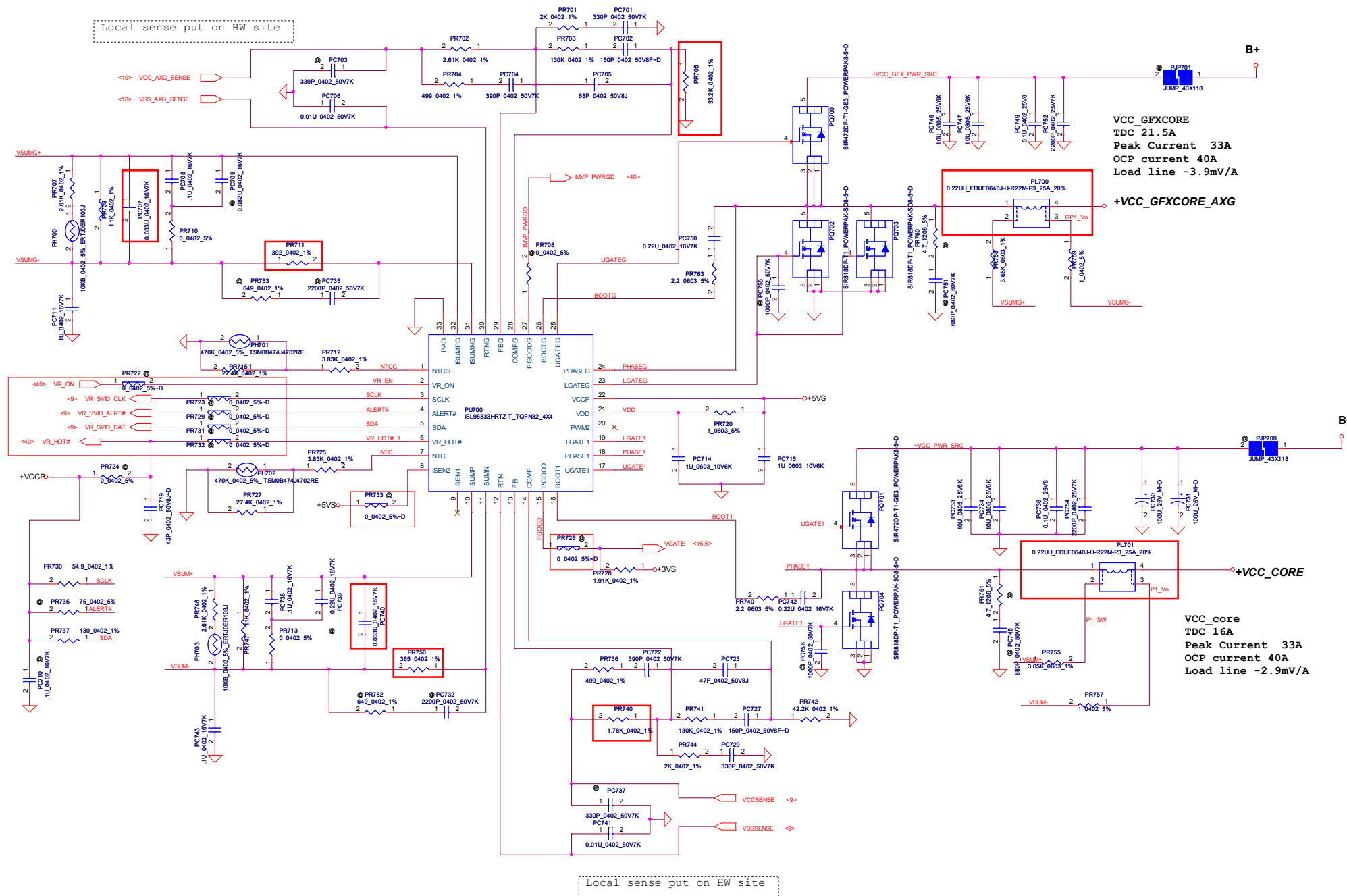


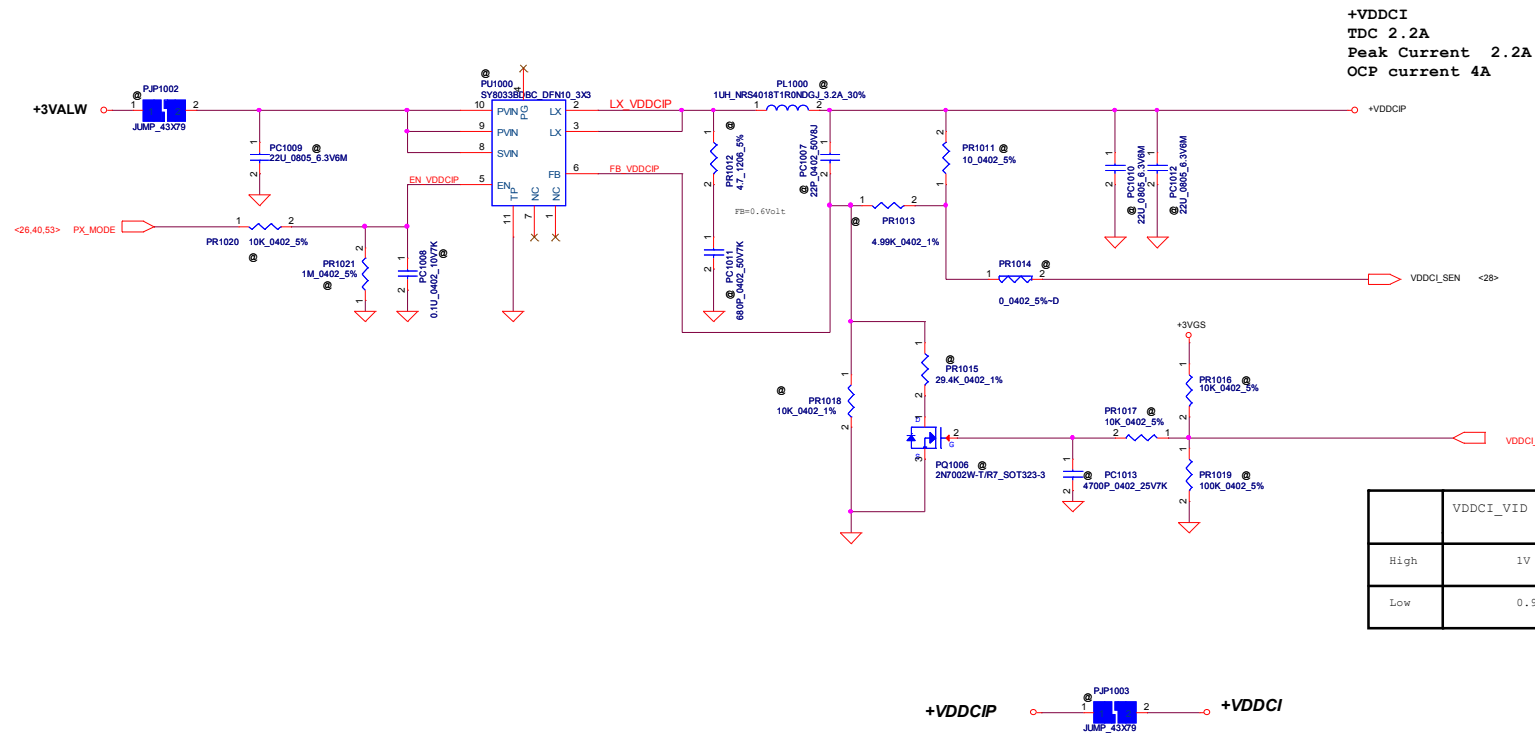
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

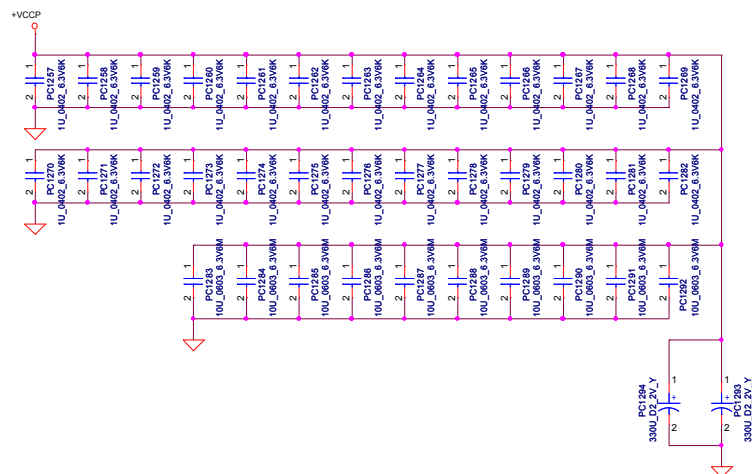
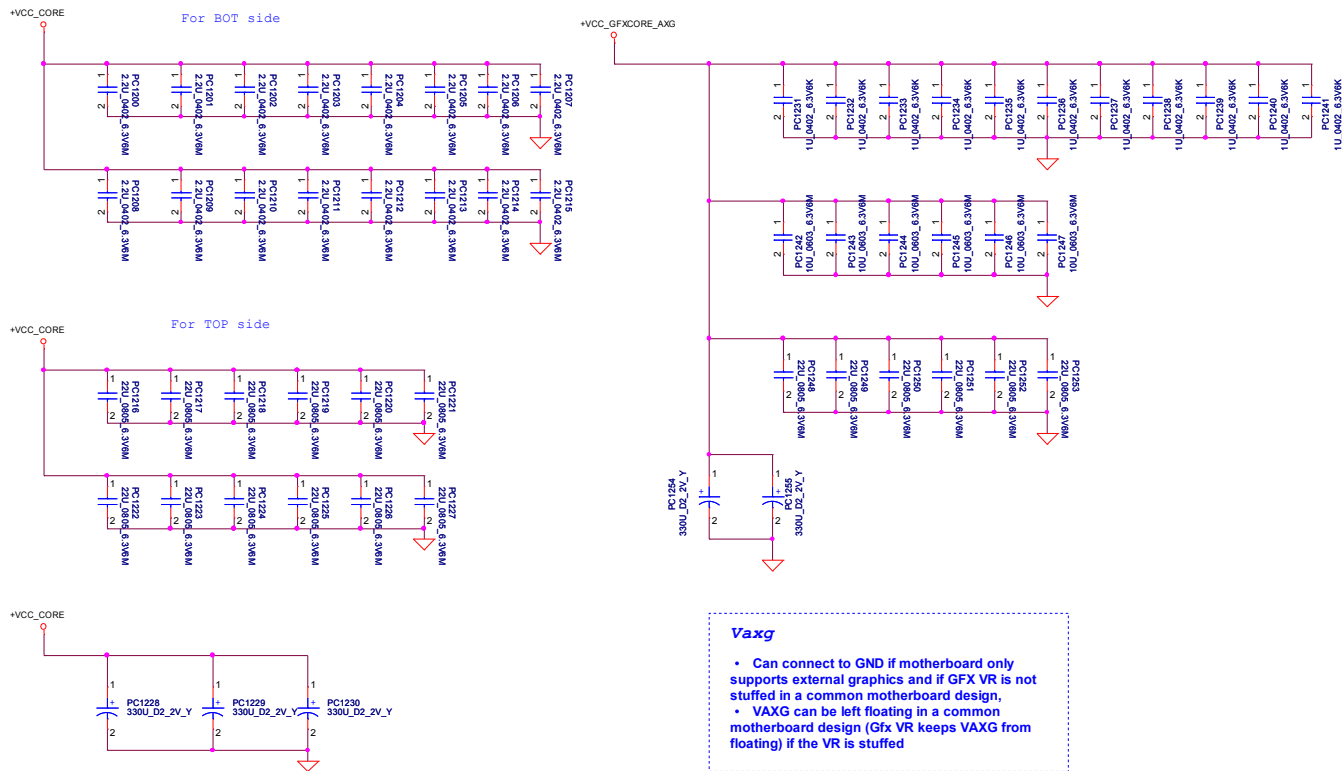


reserve for Pentium and Celeron only

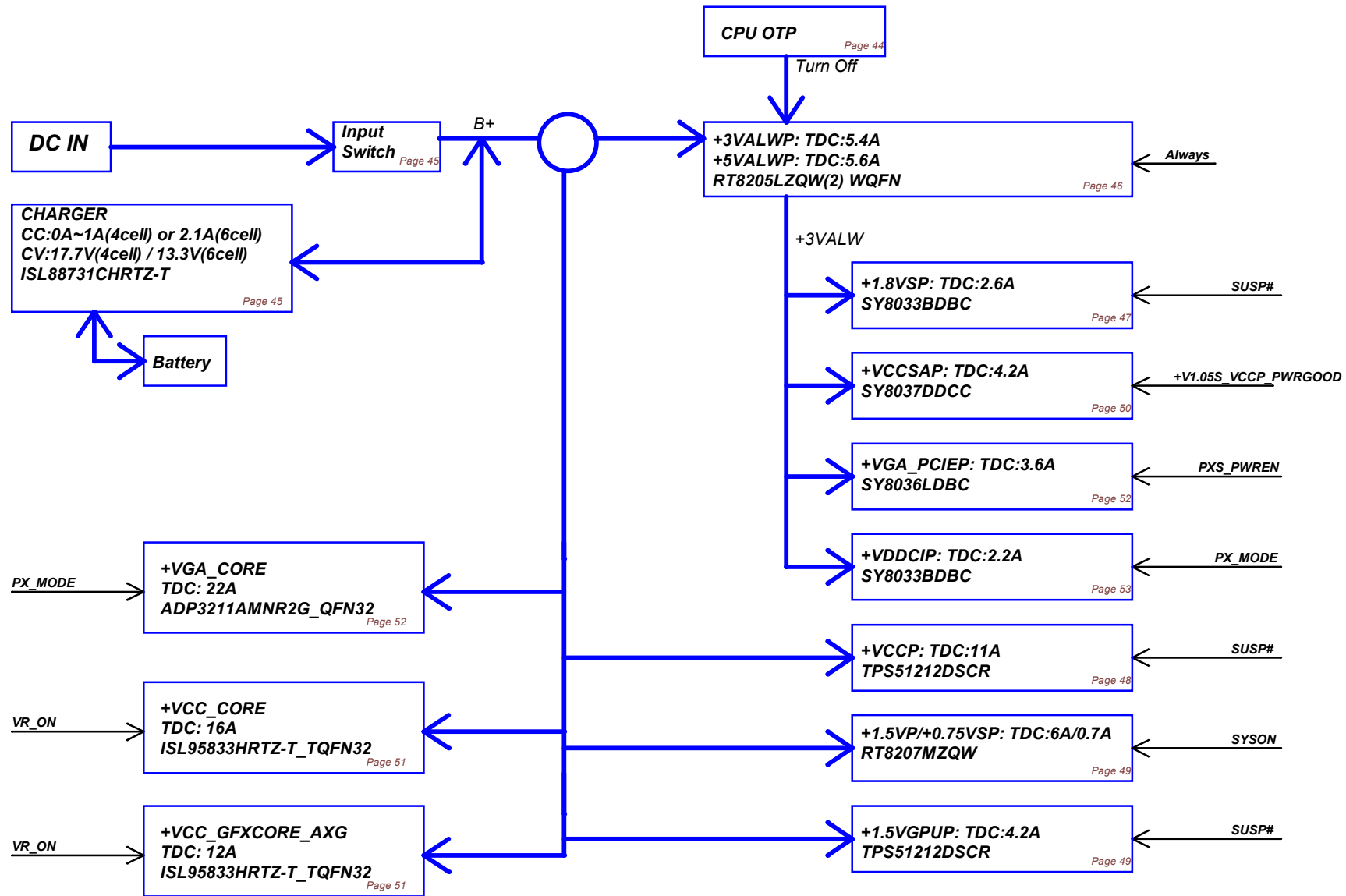
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Power block



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